On attaching acoustic imaging instrumentation to t LEO-15 observatory for sediment transport and bot boundary layer studies

Irish, J.D. Hay, A.E. Traykovski, P. Newhall, A. Craig, R. Paul, W.M.
Woods Hole Oceanogr. Instn., MA;

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INSPEC Accession Number: 7297609

Abstract:
The Woods Hole Oceanographic Institution (WHOI) and Dalhousie University conducted a sediment transport study at the LEO-15 observatory maintained Rutgers University and WHOI engineers off the central New Jersey coast. This study was designed to take advantage of the unique capabilities (power and telemetry) provided at the site. The various sensing systems were attached t bottom-mounted frame and connected by divers to the underwater-mateable ports on the LEO-15 node. The node supplied power for the various acoustic a electronic systems and provided telemetry for control of the remote instrumentation and acquisition of several GBytes of data per day. A shore-ba support station of several PCs and workstations networked together and conn to the Internet was set up at Rutgers Tuckerton Field Station to receive, displ and store this data. Instrumentation was deployed in mid-November 1999, remained active until Christmas 1999, and was recovered in January 2000. Tl methodology of using the LEO-15 observatory was different from previous approaches used by the WHOI and Dalhousie sediment transport teams and h some subtle problems not obvious until the equipment was set up and utilizin observatory. A second LEO-15 node, on shore at the Tuckerton field station, facilitated testing of each subsystem and the fully integrated system before offshore deployment. One set of problems involved the node's ground fault detection system that was designed to shut down all scientific instrumentatio protect the node when a current leak to seawater was detected on any power telemetry line. WHOI connected all their sensing systems together to provide optimum test of any system problem. Dalhousie had isolated their instrument (power and communications) so the ground fault circuit only tested the cable: the LEO-15 node to their electronics. The WHOI instrumentation developed a

slowly increasing ground fault in one line that resulted in some unnecessary c loss. The underwater-mateable connectors required at the LEO-15 sometimes showed a low ground fault level leakage that disappeared when they were reconnected. Because or the constant power source, the electronics on the tri remained powered up and active during the deployment, and individual sensc were powered and burst-sampled once or twice an hour, collecting ~4 GBytes data per day that was telemetered to shore. WHOI's high-speed link operatec successfully at ~400 kbits/sec and Dalhousie's at 2 Gb/s. Dalhousie experien some problems with their remote system suddenly stopping that may be assc with changes made to interface it with the LEO-15 observatory. All data were archived at the Tuckerton facility as the Internet link to WHOI and Dalhousie only provide 1/3 of the required speed to transmit the data collected daily. In of these problems, the systems worked much of the time and collected many gigabytes of data on the suspended sediment transport and structure in relationship to bedform roughness, and wave and current forcing. Real-time s functionality and data acquisition operations were monitored over the Interne goal of plugging instruments into the LEO-15-node and obtaining continuous time-series remotely with no interruptions is not yet fully realized. Someone l monitor the connection to keep systems functioning optimally. However, we l much of the methodology to move toward full remote operations in the future which will improve future observatories, such as the new Martha's Vineyard C Observatory

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Index Terms:
acoustic imaging earthing marine systems marine telemetry oceanographic equipm optical fibre telemetry power supplies to apparatus power system faults power syster protection sedimentation sonar imaging Internet LEO-15 observatory WHOI instrumentation Woods Hole Oceanographic Institution acoustic imaging instrumentati bottom boundary layer studies control current leak data acquisition operations data ground fault circuit ground fault detection system remote system sediment transport functionality shore-based support station telemetry underwater-mateable connectors underwater-mateable guest ports

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1 **On attaching acoustic imaging instrumentation to the LEO-15 observ for sediment transport and bottom boundary layer studies**
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[Abstract] [PDF Full-Text (417 KB)] **IEEE JNL**

2 **RF modeling of vertical interconnection between power-ground plan combined with 2D TLM**
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4 **A Wilkinson power divider on a low resistivity Si substrate with a pol**

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Radio Frequency Integrated Circuits (RFIC) Symposium, 2002 IEEE , 2-4 June :
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5 **A Wilkinson power divider on a low resistivity Si substrate with a pol interface layer for wireless circuits**
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5 **Current-source parallel-resonant DC/AC inverter with transformer**
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9 **Current-source parallel-resonant DC/AC inverter with transformer**
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[Abstract] [PDF Full-Text (424 KB)] **IEEE CNF**

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Soft-switching single-stage power factor correction converter

Rustom, K. Batarseh, I.
Sch. of Electr. Eng. & Comput. Sci., Central Florida Univ., Orlando, FL, USA;
This paper appears in: **Power Electronics Specialists Conference, 2001. I 2001 IEEE 32nd Annual**

Meeting Date: 06/17/2001 - 06/21/2001
Publication Date: 17-21 June 2001
Location: Vancouver, BC Canada
On page(s): 314 - 320 vol. 1
Volume: 1
Reference Cited: 5
Number of Pages: 4 vol. (xxxiv+2228)
Inspec Accession Number: 7138601

Abstract:
A single-stage, ZVT-PWM, **power** factor correction converter is proposed in th Zero-voltage **switching** for the main **switch** and zero-current **switching** for auxiliary **switch** are realized by utilizing the leakage inductance of the output transformer and the capacitance of the **switches**. As a result, no additional r components need to be added. ZVS operation is realized for a wide range of **l** line. High frequency operation of the proposed converter makes the AC-DC **p** supply possible to be minimized in size and weight and the soft **switching** sc reduces the electromagnetic interference (EMI). The proposed converter uses **grounded** auxiliary **switch** so that the **isolated** driving circuit is not require simplified driving circuitry again improves the overall efficiency and **power** de Practically, the direct driving schemes of both the main and the auxiliary **swit** allows the proposed converter to operate in even high **switching** frequency a good regulation capability. A 50-W 500-kHz prototype has been built in the la experimentally verify the analysis and simulation results

Index Terms:
AC-DC **power** convertors PWM **power** convertors capacitance driver circuits elec interference inductance interference suppression **power** factor correction **power** s apparatus **switching** circuits transformers 50 W 500 kHz AC-DC **power** supply reduction ZVT-PWM converter capacitance direct driving schemes electromagnet

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reduction **grounded** auxiliary **switch** **isolated** driving circuit leakage inductance c transformer **power** density simplified driving circuitry single-stage **power** factor corr converter soft-**switching** converter zero-current **switching** zero-voltage **switching**

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L5: Entry 2 of 8 File: USPT Aug 5, 2003

DOCUMENT-IDENTIFIER: US 6603221 B1
TITLE: Solid state electrical switch

Brief Summary Text (33):
Another advantage of the present invention is a state-latched control contact panels which retain the "ON" or "OFF" state after contact by the external agent is broken. Based on this latch function, the Liu Switch of the present invention provides a multipoint random remote control system, including: (a) a 2-terminal Liu Switch coupled in series with a load circuit between two lines of an AC power outlet; (b) an optocoupler coupled to the Liu Switch, the optocoupler providing a very high electrical isolation between the AC power lines and an external remote control signal bus from which the optocoupler receives input signals; and (c) controllers (e.g., computers) coupled to the signal bus, each capable of asserting on the signal bus the control signals. The Liu Switch provides an "ON/OFF" latching feature which allows random control by an unlimited number of external controllers and computers. In one implementation, the signal bus include an independent external common ground to which both the "ON" signal and the "OFF" signal reference. In another implementation, separate independent external common ground references are provided for separate transmission and isolation between "ON"-channel and "OFF"-channel on a four-wire external signal bus.

Current US Cross Reference Classification (1):
307/130

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L5: Entry 2 of 8 File: USPT Aug 5, 2003

US-PAT-NO: 6603221
DOCUMENT-IDENTIFIER: US 6603221 B1

TITLE: Solid state electrical switch

DATE-ISSUED: August 5, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liu; Zhongdu	San Jose	CA	95101	

APPL-NO: 09/ 348980 [PALM]
DATE FILED: July 7, 1999

PARENT-CASE:
CROSS-REFERENCE TO RELATED PATENT APPLICATIONS This patent application is related to and claims priority of U.S. Provisional Patent Application Serial No. 60/130,919, filed on Apr. 22, 1999 entitled "Solid State Electrical Switch", also owned by the inventor of this patent application.

INT-CL: [07] H01 H 47/00

US-CL-ISSUED: 307/125; 307/130, 307/131
US-CL-CURRENT: 307/125; 307/130, 307/131

FIELD-OF-SEARCH: 307/125, 307/130, 307/131, 327/452, 327/455, 327/469, 327/476

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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☐	3676685	July 1972	Myer	307/117
☐	3679910	July 1972	Williams	307/252W
☐	3723815	March 1973	Ambler et al.	361/45
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FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
1 052 776	November 2000	EP	
2000-357955	December 2000	JP	

ART-UNIT: 2182

PRIMARY-EXAMINER: Fleming; Fritz

ABSTRACT:

A 2-terminal solid state electrical switch is provided which can be connected in series with a load device in a the same manner as a conventional mechanical-contact switch, does not leak current during an "OFF" state, and operates from a dynamic pulse run mode during an "ON" state. The two-terminal solid state electrical switch of the present invention requires neither a power supply to operate, nor any mechanical movement and contact points. Consequently, no spark, arc or any mechanical noise is created in the solid state electrical switch's operation, nor does it corrode, thus allowing it to be used in a hostile environment. The solid state switch of the present invention can be put to uses not practical for conventional mechanical-contact switches, such as to control multi-appliances, as static circuit breakers, contactors and relays for fire-proof, explosion-proof, water-proof, anti-chemical, anti-corrosion, humidity resistant, dust resistant, anti-vibrations and heavy duty frequently operations. Further, a unique initialization circuit in the solid switch of the present invention resets the switch intelligently to a suitable operating mode after a power interruption, thus avoiding accidents that may endanger property and lives. The present invention also provides a highly isolated multi-point random remote control switch/relay suitable

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for wide industrial and other applications.

86 Claims, 27 Drawing figures

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L5: Entry 3 of 8 File: USPT Jul 2, 2002

DOCUMENT-IDENTIFIER: US 6414404 B1
TITLE: Power switching circuit

Detailed Description Text (31):
In the interest of cost and of compactness, it is desirable for all of the elements (excluding the load L which forms part of the circuit only in use) shown in the circuit of FIG. 1 or the circuit of FIG. 2 to be integrated into a single semiconductor chip. As explained in U.S. Pat. No. 5,081,379, especially for automotive applications, the voltage between the power supply lines 2 and 3 may be of the order of 50 to 60 volts. Low power logic transistor N1 to N3 such as IGFETs and the like may be integrated into the same semiconductor body as the power semiconductor switch M by providing complex structural arrangements which isolate the low power logic circuitry from the high side power semiconductor switch M. The integration involves the provision of special diffusions or barrier layers of differing conductivity types to interpose high breakdown voltage reverse bias pn-junctions between the substrate 100b to which the high voltage is applied and the low power logic devices, or by the provision of dielectric isolation. Such expensive, technically complex techniques can, however, be avoided by, as described in U.S. Pat. No. 4,929,884, operating the logic devices, with respect to the positive power supply line 2 (that is high side) rather than the earth or ground power supply line 3.

Current US Original Classification (1):
307/130

L11: Entry 8 of 26 File: USPT Jun 30, 1998

DOCUMENT-IDENTIFIER: US 5774322 A
TITLE: Three wire power supply circuit

Abstract Text (1):
A power supply circuit is provided for use in combination with a load and an alternating current (AC) power source for selectively connecting and disconnecting the load and the AC power source. The load is connected between a neutral conductor of the AC power source and the power supply circuit. The power supply circuit is connected to a power or hot line conductor and a ground conductor of the AC power source. The power supply circuit comprises relay connected in series between the load and the line conductor; a control circuit for selectively operating the relay; and a transformer. The primary winding of the transformer is connected in series with the line conductor and the ground conductor for supplying power to the control circuit even when the load is disconnected from the AC power source. The power supply circuit comprises a switch in series with the primary winding of the potential transformer for interrupting the primary winding current at frequencies above the AC line frequency. The power supply circuit can also comprise a slide or air gap switch to isolate the power supply circuit from the AC power source when the air gap switch is in the OFF position or to limit current to an acceptable level. The air gap switch can be configured to pulse the primary winding current above the accepted level.

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L13: Entry 1 of 1 File: USPT Mar 9, 1999

DOCUMENT-IDENTIFIER: US 5881251 A
TITLE: Hot swap control circuit

Abstract Text (1):
A circuit board having a load is inserted into a chassis of a digital system while the system remains in operation. During insertion, a ground potential is provided to the circuit board. Next, one or more voltage potentials are provided, however, no electrical path is provided from the voltage potentials, through the load, to ground. An enhancement voltage is provided to the circuit board, allowing the load to charge. Finally, a backplane is connected to the circuit board after the load has charged. The circuit board includes a soft start circuit that allows the load to charge gracefully after the enhancement voltage is provided. In one embodiment, the soft start circuit includes an RC circuit connected to a switch which gradually turns on as the RC circuit charges, thereby providing an electrical path from the circuit board load to ground through the switch. The switch may be a MOSFET. Once the circuit board load is charged, connecting the backplane bypasses the MOSFET, thereby eliminating nearly all quiescent current flow through, and associated power dissipation in, the MOSFET. The circuit board is extracted from the chassis of the digital system by first disconnecting the backplane. When this occurs, the MOSFET is no longer bypassed by the backplane connection and quiescent current again flows through the MOSFET. Next, the enhancement voltage is removed, allowing the MOSFET to gradually turn off as the RC circuit discharges, thereby removing the electrical path from the load to ground. The voltage and ground potential are then removed.

Brief Summary Text (10):
The circuit board includes a soft start circuit to allow the circuit board to charge gracefully after the enhancement voltage is provided. In one embodiment, the soft start circuit includes an RC circuit which charges over a predetermined time after the enhancement voltage is provided. The RC circuit is connected to a switch which gradually turns on as the RC circuit charges, thereby providing an electrical path from the circuit board load to ground through the switch. In one embodiment, the switch is a MOSFET having a current rating appropriate to the quiescent circuit board load current. Once the circuit board load is charged, connecting the backplane bypasses the MOSFET, thereby eliminating nearly all current flow through, and associated power dissipation in, the MOSFET.

Detailed Description Text (3):
FIG. 1 illustrates a digital system 5 configured in accordance with the present invention. Digital system 5 includes a chassis 10 and a circuit board 20. Chassis 10 includes a ground post 30, power posts 31, a soft start post 32, and a backplane connector 33. Circuit board 20 includes a ground connector 40, power connectors 41, a soft start connector 42, a backplane coupling 43, a switch circuit 50, and board loads 60. Circuit board 20 may be inserted into or extracted from chassis 10 at any time, without having to power down the digital system 5.

Detailed Description Text (5):
Insertion of circuit board 20 into chassis 10, should be carried out in a controlled manner. Ground post 30 on chassis 10 is first coupled with the ground

connector 40 on circuit board 20 in order to facilitate electrostatic discharge of the circuit board 20. Next, power post(s) 31 on chassis 10 is/are coupled with power connector(s) 41 on circuit board 20. Each power connector 41 is coupled to a respective circuit board load 60. Circuit board loads 60 represent the equivalent circuit loads for the various circuits located on circuit board 20. Notice that even though power posts 31 are connected to power connectors 41, no current flows across circuit board loads 60 because switch circuit 50 acts as an open circuit, preventing a path from the circuit board loads 60 to ground.

Detailed Description Text (7):
As MOSFET 52 switches on, circuit board loads 60 are provided with a path to ground post 30. Those skilled in the art will recognize that MOSFET 52 is current rated depending upon the magnitude of the quiescent circuit board loads 60. After circuit board loads 60 are charged, and as circuit board 20 is further inserted into chassis 10, backplane connector 33 on chassis 10 is coupled to backplane coupling 43 on circuit board 20. Backplane coupling 43 on circuit board 20 and backplane connector 33 on chasis 10 provide a current path which bypasses MOSFET 52. As a result, even though MOSFET 52 remains turned on, there is little or no further power dissipation in MOSFET 52.

Detailed Description Text (8):
Extraction of circuit board 20 from chassis 10 should also be carried out in a controlled manner. During extraction, backplane connector 33 is first disconnected from backplane coupling 43 and quiescent current again begins to flow through MOSFET 52 to ground post 30. As extraction of circuit board 20 continues, soft start post 32 is disconnected from soft start connector 42. Disconnecting soft start post 32 in this fashion causes RC circuit 54 to discharge through resistor circuit 56, allowing circuit board load 60 to power down gracefully as MOSFET 52 switches off. As the extraction process continues, power posts 31 are disconnected from power connectors 41, removing all voltage from circuit board 20. After power posts 31 are disconnected, ground post 30 is disconnected from ground connector 40, completing the extraction of circuit board 20 from chassis 10.

Current US Original Classification (1):
710/302

CLAIMS:

12. A method of removing a circuit board having a circuit board load from a chassis comprising the steps of:

disconnecting a backplane from the circuit board;

removing an enhancement voltage from the circuit board by terminating a quiescent current flow from the circuit board load through a switch to an electrical ground in a controlled fashion, the circuit board thus being configured to allow the circuit board load to power down gracefully once the enhancement voltage is removed;

removing one or more voltage potentials from the circuit board once the circuit board load has powered down; and

removing a ground potential from the circuit board only after all other voltage potentials have been removed therefrom.

First Hit Fwd Refs

End of Result Set

☐ Generate Collection Print

L13: Entry 1 of 1 File: USPT Mar 9, 1999

US-PAT-NO: 5881251
DOCUMENT-IDENTIFIER: US 5881251 A

TITLE: Hot swap control circuit

DATE-ISSUED: March 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fung; Laurie P.	Pleasanton	CA		
Lindberg; Craig D.	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Bay Networks, Inc.	Santa Clara	CA			02

APPL-NO: 08/ 728202 [PALM]
DATE FILED: October 10, 1996

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/283; 307/147
US-CL-CURRENT: 710/302; 307/147

FIELD-OF-SEARCH: 395/283, 395/282, 395/281, 307/147, 307/148

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5432916	July 1995	Hahn et al.	395/283
☐	5473499	December 1995	Weir	395/283
☐	5530810	June 1996	Bowman	395/283
☐	5584030	December 1996	Husak et al.	395/283
☐	5625238	April 1997	Ady et al.	395/283
☐	5636347	June 1997	Muchnick et al.	395/283
☐	5644731	July 1997	Liencres et al.	395/283

h e b b g e e e f c e b e ge

☐	5726506	March 1998	Wood	307/147

ART-UNIT: 271

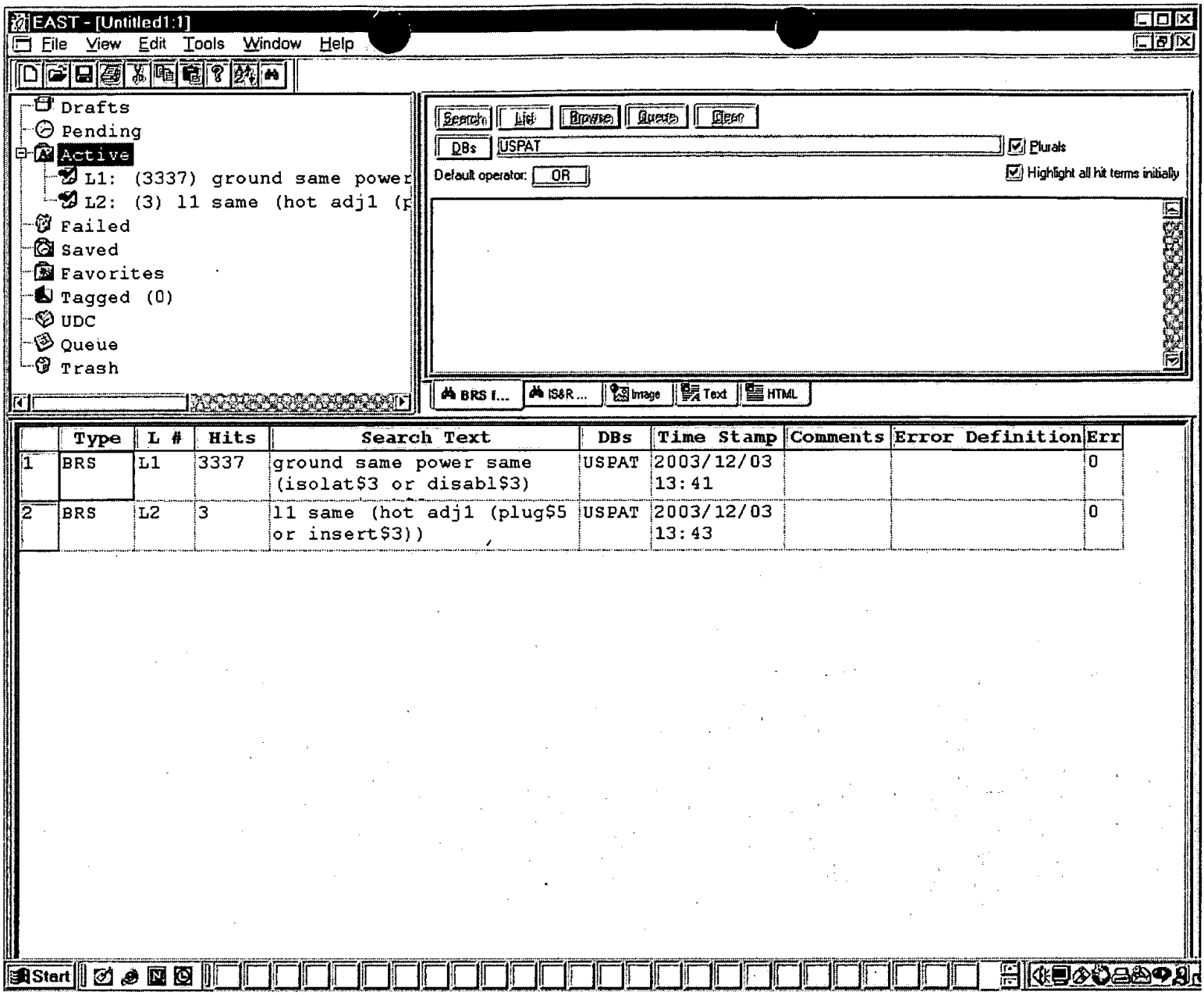
PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Blakely Sokoloff Taylor & Zafman, LLP

ABSTRACT:

A circuit board having a load is inserted into a chassis of a digital system while the system remains in operation. During insertion, a ground potential is provided to the circuit board. Next, one or more voltage potentials are provided, however, no electrical path is provided from the voltage potentials, through the load, to ground. An enhancement voltage is provided to the circuit board, allowing the load to charge. Finally, a backplane is connected to the circuit board after the load has charged. The circuit board includes a soft start circuit that allows the load to charge gracefully after the enhancement voltage is provided. In one embodiment, the soft start circuit includes an RC circuit connected to a switch which gradually turns on as the RC circuit charges, thereby providing an electrical path from the circuit board load to ground through the switch. The switch may be a MOSFET. Once the circuit board load is charged, connecting the backplane bypasses the MOSFET, thereby eliminating nearly all quiescent current flow through, and associated power dissipation in, the MOSFET. The circuit board is extracted from the chassis of the digital system by first disconnecting the backplane. When this occurs, the MOSFET is no longer bypassed by the backplane connection and quiescent current again flows through the MOSFET. Next, the enhancement voltage is removed, allowing the MOSFET to gradually turn off as the RC circuit discharges, thereby removing the electrical path from the load to ground. The voltage and ground potential are then removed.

27 Claims, 3 Drawing figures



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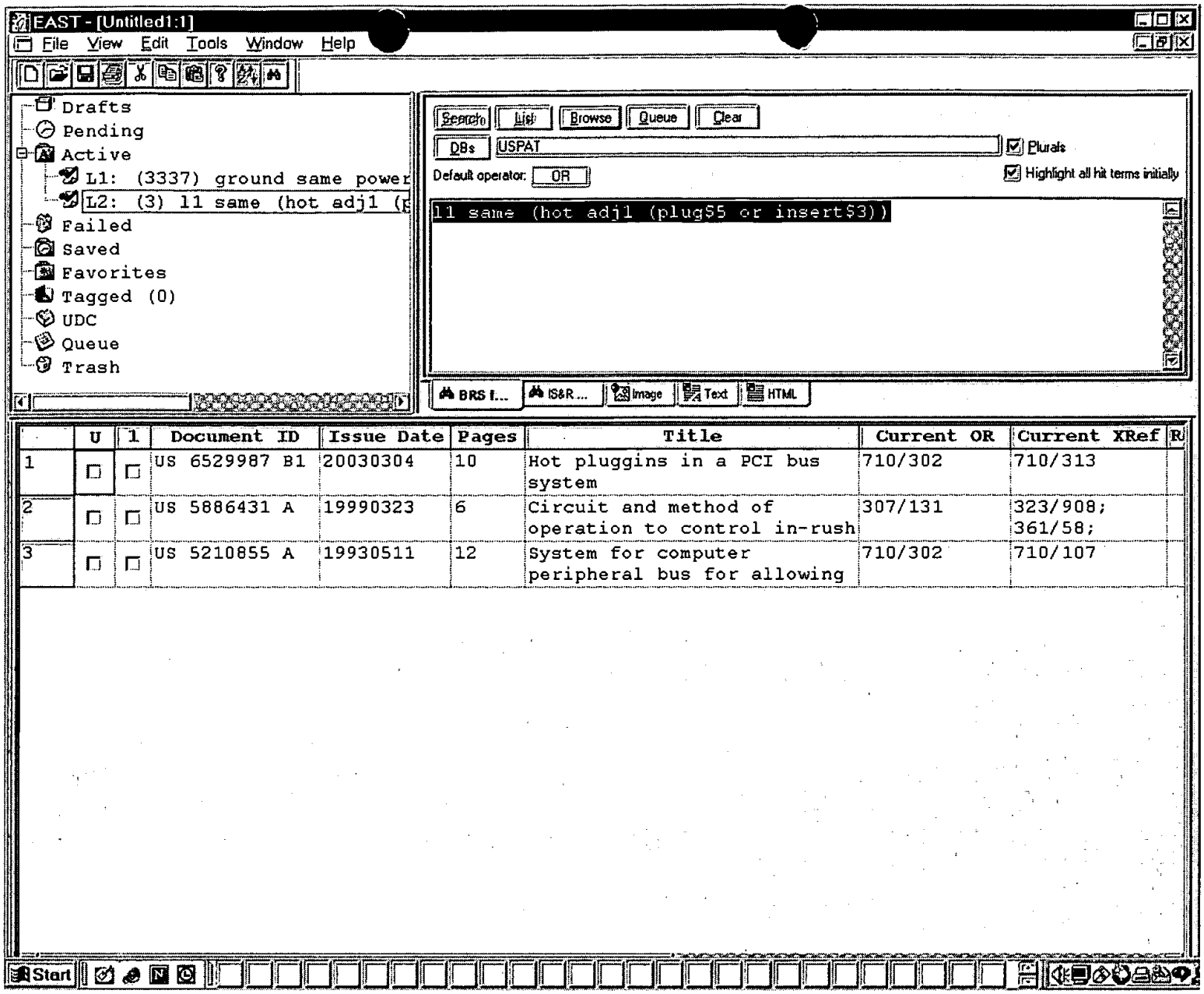
2	BRS	L2	3	l1 same (hot adj1 (plug$5 or insert$3))	USPAT	2003/12/03 13:43			0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File View Edit Tools Window Help
Drafts
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Active
L1: (3337) ground same power
L2: (3) 11 same (hot adj1 (
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Plurals
Default operator:
OR
Highlight all hit terms initially
11 same (hot adj1 (plug$5 or insert$3))
BRS I...
IS&R ...
Image
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1
Document ID
Issue Date
Pages
Title
Current OR
Current XRef
1
US 6529987 B1
20030304
10
Hot pluggins in a PCI bus system
710/302
710/313
2
US 5886431 A
19990323
6
Circuit and method of operation to control in-rush
307/131
323/908; 361/58;
3
US 5210855 A
19930511
12
System for computer peripheral bus for allowing
710/302
710/107
Start

US-PAT-NO: 4703407

DOCUMENT-IDENTIFIER: US 4703407 A

TITLE: Power supply for totem pole power switches

---------- KWIC ---------

Brief Summary Text - BSTX (7):

The present invention solves the aforementioned problems associated with the prior art as well as other problems by providing an improved power supply system for power switches arranged in a totem pole circuit configuration. The improved power supply system involves a single power supply having an output voltage that is substantially less than the voltage applied to the upper power switch and a flying capacitor circuit which is charged to the output voltage of the power supply. Microprocessor based control circuitry provides the logic necessary to control the upper and lower power switches and regulates the charging of a capacitor in the flying capacitor circuit. A ground isolation circuit isolates the microprocessor based control circuitry from the voltage that is applied to the upper power switch. Actuation of the lower power switch and the deactuation of the upper power switch causes the capacitor to be charged by the power supply resulting in the output of the power switches to be maintained at the system common. Conversely, actuation of the upper power switch and deactuation of the lower power switch causes the capacitor to discharge through its load so as to maintain a voltage at the output of the power switches equal to the voltage applied to the upper power switch.

United States Patent [19]

Fry et al.

[11] **Patent Number: 4,703,407**

[45] **Date of Patent: Oct. 27, 1987**

[54] **POWER SUPPLY FOR TOTEM POLE POWER SWITCHES**

[75] Inventors: John J. Fry, Wickliffe; Edward Bastijanic, Concord; John W. Robertson, Jr., Chesterland, all of Ohio

[73] Assignee: The Babcock & Wilcox Company, New Orleans, La.

[21] Appl. No.: 935,351

[22] Filed: Nov. 26, 1986

[51] Int. Cl.[4] H02M 3/335

[52] U.S. Cl. 363/16; 323/271; 320/1

[58] Field of Search 363/16-17; 323/268, 271; 320/1; 307/500, 255, 288, 313

[56] References Cited

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4,395,675	7/1983	Toumani	323/271

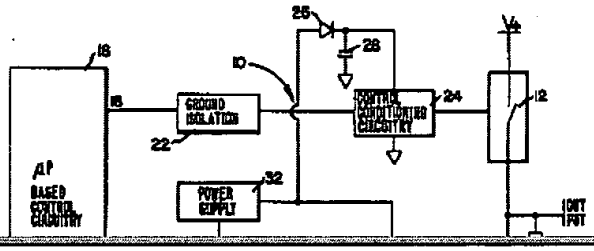
Primary Examiner—Peter S. Wong

Attorney, Agent, or Firm—Vytas R. Matas; Robert J. Edwards

[57] **ABSTRACT**

An improved power supply for power switches arranged in a totem pole configuration is disclosed. A single power supply, having an output voltage substantially less than the voltage applied to the upper power switch, periodically charges a capacitor within a flying capacitor circuit. Microprocessor based control circuitry controls the charging and discharging of the capacitor and the periodic operation of the power switches resulting in the voltage at the output of the power switches being at system common or at the voltage applied to the upper power switch.

8 Claims, 1 Drawing Figure



US-PAT-NO: 5434509

DOCUMENT-IDENTIFIER: US 5434509 A

TITLE: Method and apparatus for detecting arcing in alternating-current power systems by monitoring high-frequency noise

---------- KWIC ---------

Detailed Description Text - DETX (70):

As shown in FIG. 9, the main power lines, consisting of high 107, neutral 108 and ground 106 conductors, provide power to the load through a switch element 111 controlled by a solenoid 113 of a conventional circuit breaker (i.e., also providing overcurrent protection) to high, neutral, and ground conductors 112,116, and 117, respectively. The high line is routed through a current transformer 109 having a pass band of 1-10 MHz, that monitors current to the load. A zero-detection circuit is used to monitor the line voltage if it is desired to have the same device operable in systems having differing line frequencies, as in other countries. The current transformer 109 monitors only current flowing to the load, thereby isolating the arc detection circuit from arcs generated on the individual circuit protected by breaker 113.

US-PAT-NO: 6288916

DOCUMENT-IDENTIFIER: US 6288916 B1

TITLE: Multiple output uninterruptible alternating current power supplies for communications system

---------- KWIC ---------

Abstract Text - ABTX (1):
A UPS system for communications systems. The UPS system comprises an input stage that generates primary and standby AC power signals. The primary and standby AC power signals are passed through an isolation transformer and through an output rectifier to obtain an output DC power signal. A plurality of output inverters are used to generate a plurality of output AC power signals from the output DC power signal. A switch circuit is provided to connect one or more of the output DC power signals to one or more loads of the communications system.

US006222709B1

(12) **United States Patent**
Baba

(10) **Patent No.: US 6,222,709 B1**
(45) **Date of Patent: Apr. 24, 2001**

(54) **DEVICE AND METHOD FOR SUPPLYING ELECTRIC POWER TO A LOAD**

(75) Inventor: **Akira Baba**, Shizuoka-ken (JP)

(73) Assignee: **Yazaki Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/502,213**

(22) Filed: **Feb. 11, 2000**

(30) **Foreign Application Priority Data**

Feb. 14, 1999 (JP) 11-074260
Feb. 7, 2000 (JP) 12-029581

(51) Int. Cl.[7] H02H 7/00; G05F 1/40
(52) U.S. Cl. 361/18; 323/282
(58) Field of Search 323/282, 283, 323/285; 361/18, 87, 91, 93, 98; 320/22, 30, 39

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6-188704 7/1994 (JP).
6-244693 9/1994 (JP).
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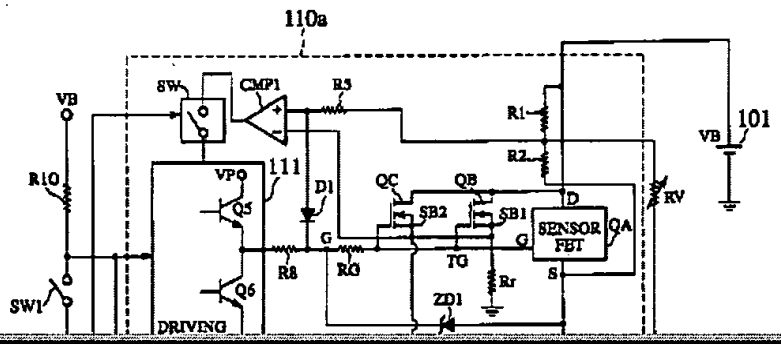
Primary Examiner—Matthew Nguyen
(74) *Attorney, Agent, or Firm*—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

(57) **ABSTRACT**

An improved electric power supply control device for supplying electric power to a load from a battery is described. The electric power supply control device is composed of a semiconductor switch connected between the electric power source and the load in order to controlling the power supply to the load, an excessive electric current detecting circuit for detecting an excessive electric current flowing through the load, a protection circuit connected to the semiconductor switch for turning off the semiconductor switch if the excessive electric current detecting circuit detects an excessive electric current, and a control circuit for disabling the protection circuit from turning off the semiconductor switch if the rate of increase of the electric current as flowing through the load is smaller than a predetermined rate.

5 Claims, 7 Drawing Sheets



US-PAT-NO: 5721657

DOCUMENT-IDENTIFIER: US 5721657 A

TITLE: Load control module

---------- KWIC ---------

Abstract Text - ABTX (1):
A load control module (1) for controlling switch gear (2) which, in use, connects a power source (3) to remotely located electrical load (4). The module (1) includes a sensor unit (9) associated with the load (4) for providing a signal indicative of predetermined operating parameters of the load and a controller (10) for receiving the signal and for selectively providing another signal to the switch gear (2) which isolates the load (4) from the power source (3) when the load (4) does not comply with required operating parameters.

US005721657A

United States Patent [19]

Griffiths et al.

[11] Patent Number: 5,721,657

[45] Date of Patent: Feb. 24, 1998

[54] LOAD CONTROL MODULE

[75] Inventors: Gregory Mark Griffiths, The Junction; Eric Gayne Gibbons, New Lambton; Roman Fidyk, Adamstown Heights; John William Weaver, Valentine, all of Australia

[73] Assignee: Metal Manufactures Limited, Sydney, Australia

[21] Appl. No.: 680,939

[22] PCT Filed: Aug. 23, 1994

[86] PCT No.: PCT/AU94/00492

§ 371 Date: Aug. 20, 1996

§ 102(e) Date: Aug. 20, 1996

[87] PCT Pub. No.: WO95/06349

PCT Pub. Date: Mar. 2, 1995

[30] Foreign Application Priority Data

Aug. 24, 1993 [AU] Australia ..... PM 0808

[51] Int. Cl.[6] H02H 3/00

[52] U.S. Cl. 361/93; 361/115; 361/78

[58] Field of Search 361/18, 93, 115, 361/42, 78

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(List continued on next page.)

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Sprecher+Schuh, Electronic Motor Protection Unit CET 3 Brochure, (Jun. 1984).

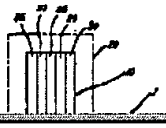
(List continued on next page.)

Primary Examiner—Brian K. Young
Assistant Examiner—Stephen Jackson
Attorney, Agent, or Firm—Leydig, Voit & Mayer, Ltd.

[57] ABSTRACT

A load control module (1) for controlling switch gear (2) which, in use, connects a power source (3) to remotely located electrical load (4). The module (1) includes a sensor unit (9) associated with the load (4) for providing a signal indicative of predetermined operating parameters of the load and a controller (18) for receiving the signal and for selectively providing another signal to the switch gear (2) which isolates the load (4) from the power source (3) when the load (4) does not comply with required operating parameters.

7 Claims, 1 Drawing Sheet



US-PAT-NO: 5118963

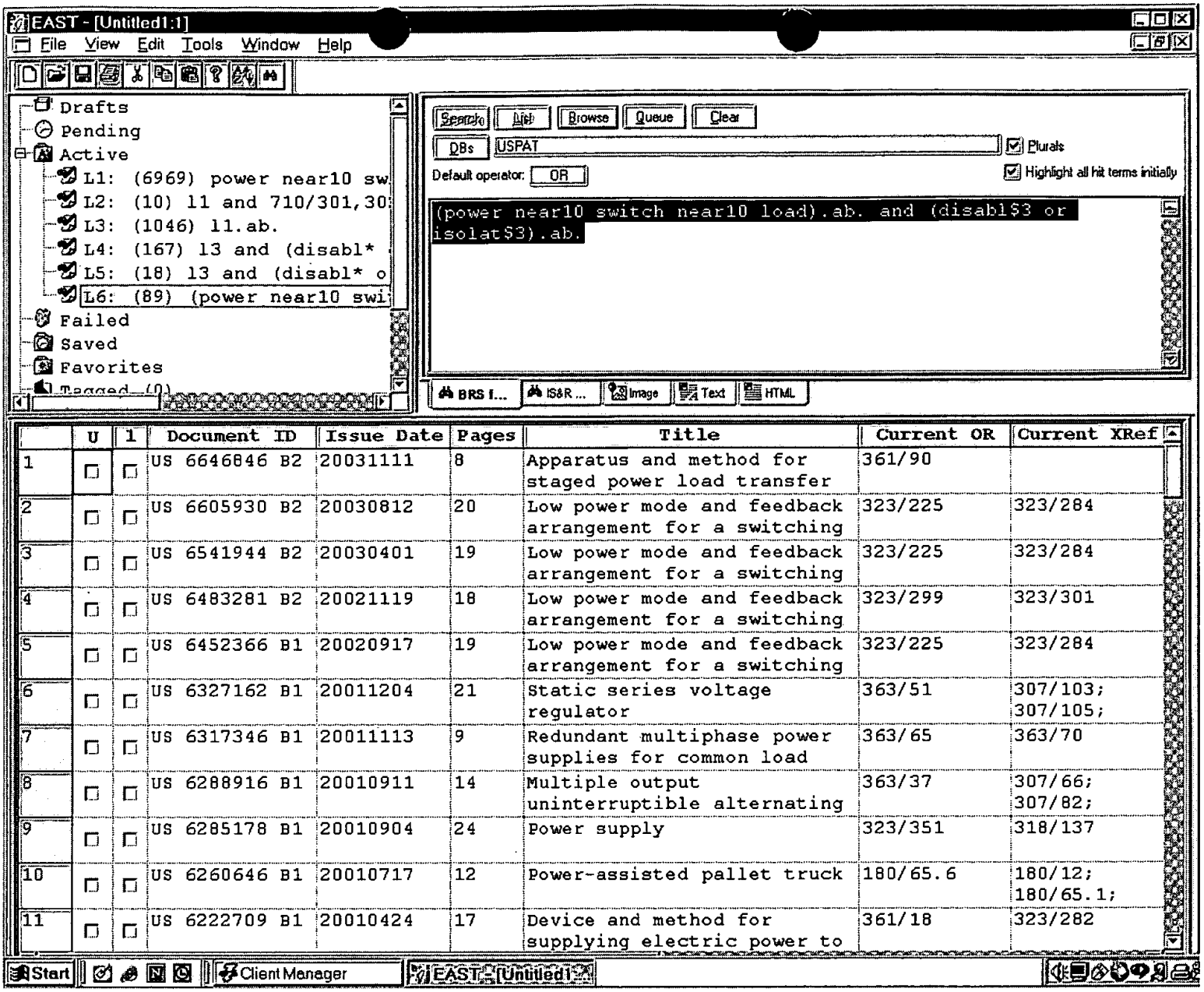
DOCUMENT-IDENTIFIER: US 5118963 A

TITLE: Symmetrical controlled switching circuit

---------- KWIC ---------

Abstract Text - ABTX (1):

A switching circuit is disclosed which provides a plurality of switches which can be caused to open or close, a controller which can selectively draw current from a plurality of power sources connected in electrical communication with the switches and isolating devices connecting the switches to the controller. The controller is connected to a regulator and to one voltage interconnection and the regulator is connected to another voltage interconnection by two conductive paths which control individual switches that are associated with individual power supplying loads.



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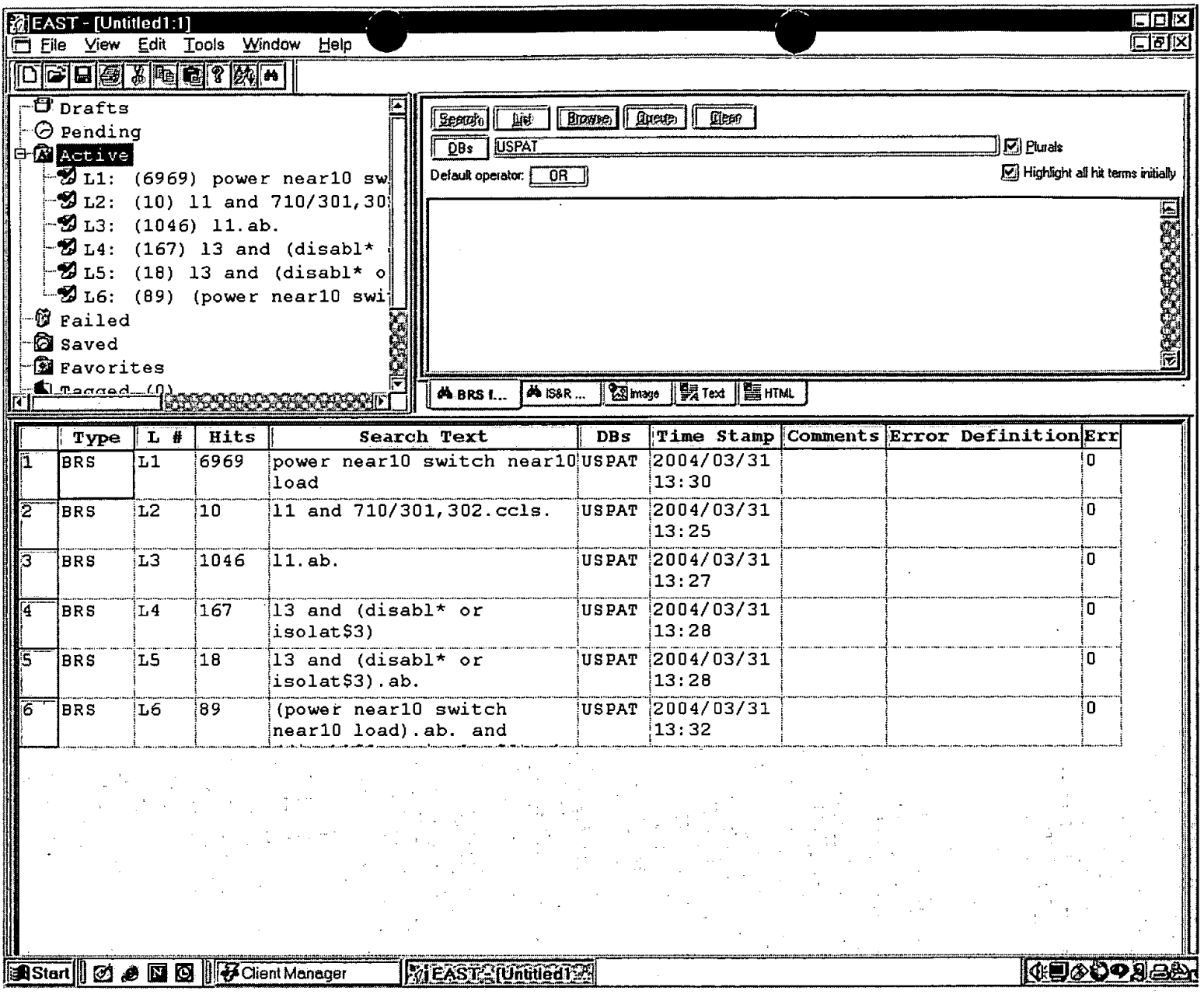
1	☐	☐	US 6646846 B2	20031111	8	Apparatus and method for staged power load transfer	361/90	
2	☐	☐	US 6605930 B2	20030812	20	Low power mode and feedback arrangement for a switching	323/225	323/284
3	☐	☐	US 6541944 B2	20030401	19	Low power mode and feedback arrangement for a switching	323/225	323/284
4	☐	☐	US 6483281 B2	20021119	18	Low power mode and feedback arrangement for a switching	323/299	323/301
5	☐	☐	US 6452366 B1	20020917	19	Low power mode and feedback arrangement for a switching	323/225	323/284
6	☐	☐	US 6327162 B1	20011204	21	Static series voltage regulator	363/51	307/103; 307/105;
7	☐	☐	US 6317346 B1	20011113	9	Redundant multiphase power supplies for common load	363/65	363/70
8	☐	☐	US 6288916 B1	20010911	14	Multiple output uninterruptible alternating	363/37	307/66; 307/82;
9	☐	☐	US 6285178 B1	20010904	24	Power supply	323/351	318/137
10	☐	☐	US 6260646 B1	20010717	12	Power-assisted pallet truck	180/65.6	180/12; 180/65.1;
11	☐	☐	US 6222709 B1	20010424	17	Device and method for supplying electric power to	361/18	323/282



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3	BRS	L3	1046	l1.ab.	USPAT	2004/03/31 13:27			0
4	BRS	L4	167	l3 and (disabl* or isolat$3)	USPAT	2004/03/31 13:28			0
5	BRS	L5	18	l3 and (disabl* or isolat$3).ab.	USPAT	2004/03/31 13:28			0
6	BRS	L6	89	(power near10 switch near10 load).ab. and	USPAT	2004/03/31 13:32			0

US006288916B1

(12) **United States Patent**
Liu et al.

(10) **Patent No.: US 6,288,916 B1**
(45) **Date of Patent: Sep. 11, 2001**

(54) **MULTIPLE OUTPUT UNINTERRUPTIBLE ALTERNATING CURRENT POWER SUPPLIES FOR COMMUNICATIONS SYSTEM**

(75) Inventors: Frank Liu; Pu Han; Lam Vu, all of Bellingham, WA (US)

(73) Assignee: Alpha Technologies, Inc., Bellingham, WA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/419,220

(22) Filed: Oct. 15, 1999

(51) Int. Cl.[7] H02M 5/45; H02J 7/00

(52) U.S. Cl. 363/37; 363/71; 307/66; 307/82

(58) Field of Search 363/34, 37, 71; 307/64, 66, 82

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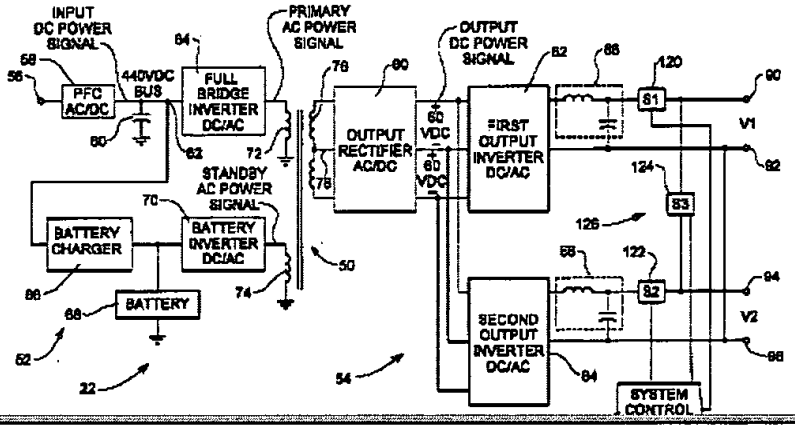
Primary Examiner—Adolf Deneke Berhane
(74) *Attorney, Agent, or Firm*—Michael B. Schacht; Hughes & Schacht, P.S.

(57) **ABSTRACT**

A UPS system for communications systems. The UPS system comprises an input stage that generates primary and standby AC power signals. The primary and standby AC power signals are passed through an isolation transformer and through an output rectifier to obtain an output DC power signal. A plurality of output inverters are used to generate a plurality of output AC power signals from the output DC power signal. A switch circuit is provided to connect one or more of the output DC power signals to one or more loads of the communications system.

15 Claims, 8 Drawing Sheets



US-PAT-NO: 6222709

DOCUMENT-IDENTIFIER: US 6222709 B1
See image for Certificate of Correction

TITLE: Device and method for supplying electric power to a load

---------- KWIC ---------

Abstract Text - ABTX (1):

An improved electric power supply control device for supplying electric power to a load from a battery is described. The electric power supply control device is composed of a semiconductor switch connected between the electric power source and the load in order to controlling the power supply to the load, an excessive electric current detecting circuit for detecting an excessive electric current flowing through the load, a protection circuit connected to the semiconductor switch for turning off the semiconductor switch if the excessive electric current detecting circuit detects an excessive electric current, and a control circuit for disabling the protection circuit from turning off the semiconductor switch if the rate of increase of the electric current as flowing through the load is smaller than a predetermined rate.

Refine Search

Search Results -

Terms	Documents
L1 same (disabl$3 or isolat$3)	385

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search | Recall Text | Clear | Interrupt

Search History

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L2	L1 same (disabl$3 or isolat$3)	385	L2
L1	switch same power same ground same load	3164	L1

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Refine Search

Search Results -

Terms	Documents
L2	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, March 31, 2004 Printable Copy Create Case

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L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 same (disabl$3 or isolat$3)	385	L2
L1	switch same power same ground same load	3164	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
(361/58 |361/686 |710/301 |710/302 |710/313 |323/908 |307/130 |307/11 |307/126 |713/300).ccls.	4217

Database:
- US Pre-Grant Publication Full-Text Database
- **US Patents Full-Text Database**
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, March 31, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L4	710/301,302,313;307/130,11,126;361/58,686;713/300;323/908.ccls.	4217	L4
DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 same (disabl$3 or isolat$3)	385	L2
L1	switch same power same ground same load	3164	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L2 and L4	8

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, March 31, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L5	l2 and L4	8	L5
L4	710/301,302,313;307/130,11,126;361/58,686;713/300;323/908.ccls.	4217	L4
DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 same (disabl$3 or isolat$3)	385	L2
L1	switch same power same ground same load	3164	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L8 or L9	7

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L10

Refine Search | Recall Text | Clear | Interrupt

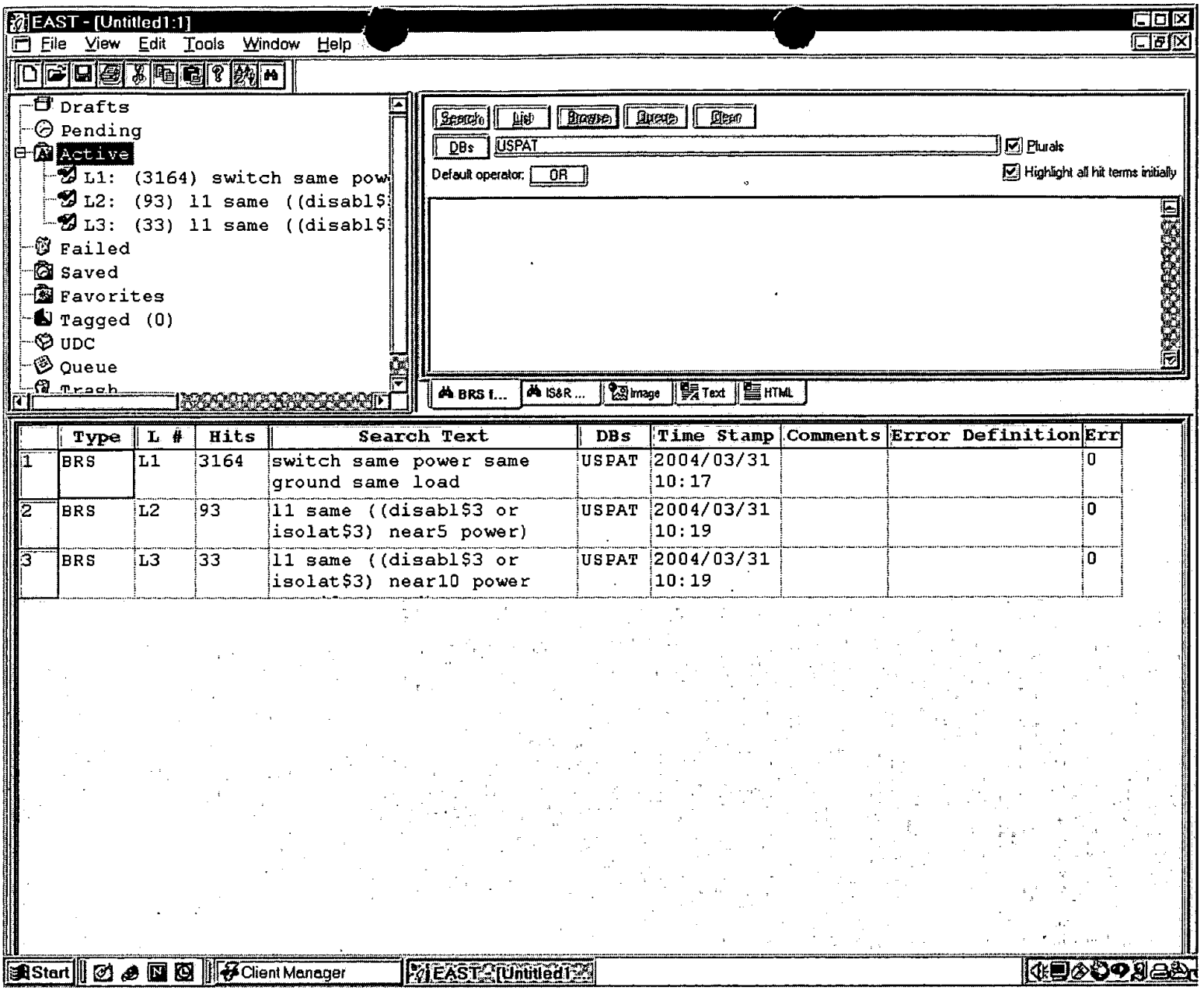
Search History

DATE: Wednesday, March 31, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L10	l8 or L9	7	L10
L9	l2 and ((hot or live) same (plug$4 or swap$5))	7	L9
L8	l2 same (hot or live) same (plug$4 or swap$5)	4	L8
L7	l2 and ((hot or live) adj1 (plug$4 or swap$5))	0	L7
L6	l2 same ((hot or live) adj1 (plug$4 or swap$5))	0	L6
L5	l2 and L4	8	L5
L4	710/301,302,313;307/130,11,126;361/58,686;713/300;323/908.ccls.	4217	L4
DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 same (disabl$3 or isolat$3)	385	L2
L1	switch same power same ground same load	3164	L1

END OF SEARCH HISTORY

h e b b cg b e e ch



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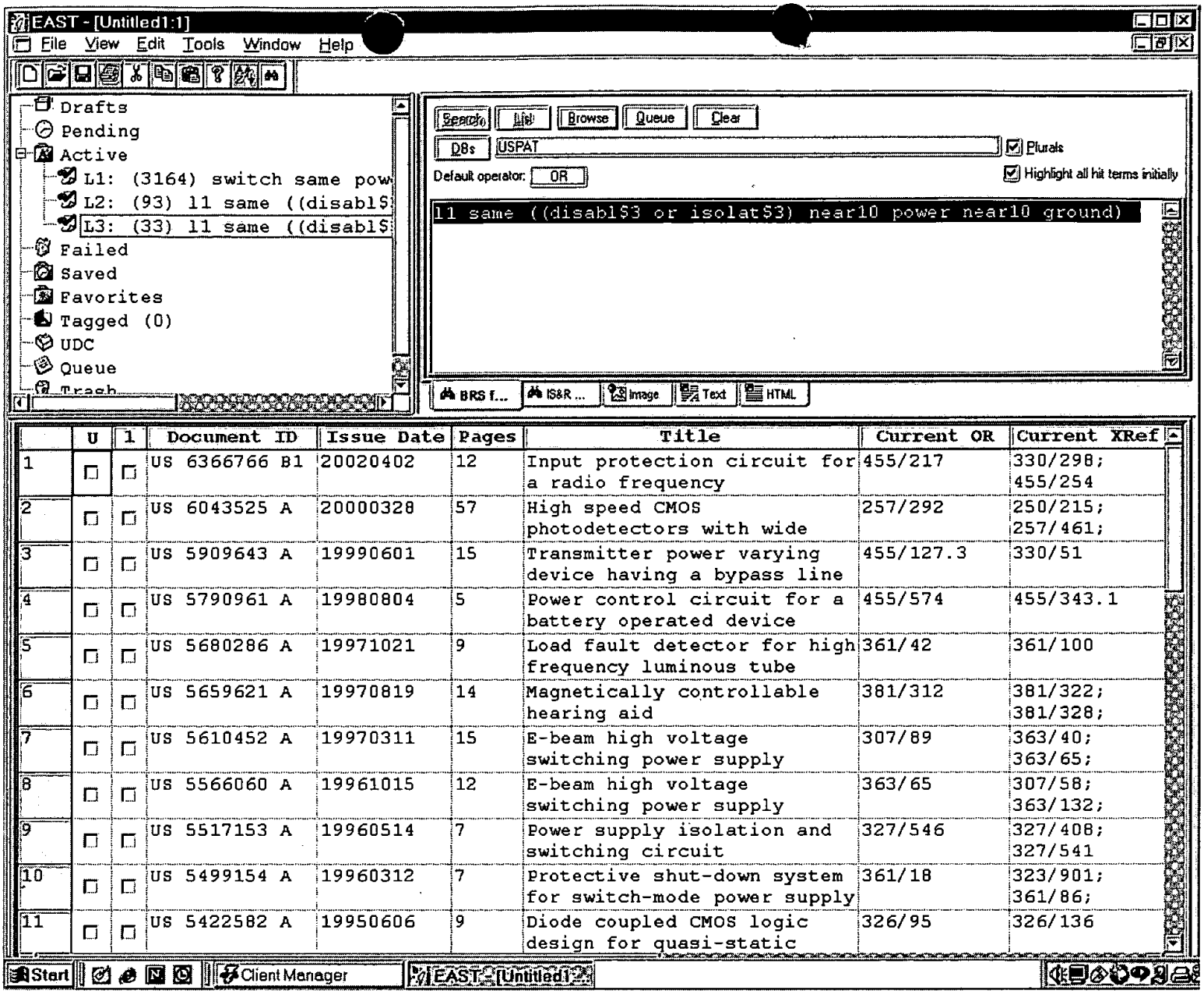
1	BRS	L1	3164	switch same power same ground same load	USPAT	2004/03/31 10:17			0
2	BRS	L2	93	l1 same ((disabl$3 or isolat$3) near5 power)	USPAT	2004/03/31 10:19			0
3	BRS	L3	33	l1 same ((disabl$3 or isolat$3) near10 power	USPAT	2004/03/31 10:19			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6366766 B1	20020402	12	Input protection circuit for a radio frequency	455/217	330/298; 455/254
2	☐	☐	US 6043525 A	20000328	57	High speed CMOS photodetectors with wide	257/292	250/215; 257/461;
3	☐	☐	US 5909643 A	19990601	15	Transmitter power varying device having a bypass line	455/127.3	330/51
4	☐	☐	US 5790961 A	19980804	5	Power control circuit for a battery operated device	455/574	455/343.1
5	☐	☐	US 5680286 A	19971021	9	Load fault detector for high frequency luminous tube	361/42	361/100
6	☐	☐	US 5659621 A	19970819	14	Magnetically controllable hearing aid	381/312	381/322; 381/328;
7	☐	☐	US 5610452 A	19970311	15	E-beam high voltage switching power supply	307/89	363/40; 363/65;
8	☐	☐	US 5566060 A	19961015	12	E-beam high voltage switching power supply	363/65	307/58; 363/132;
9	☐	☐	US 5517153 A	19960514	7	Power supply isolation and switching circuit	327/546	327/408; 327/541
10	☐	☐	US 5499154 A	19960312	7	Protective shut-down system for switch-mode power supply	361/18	323/901; 361/86;
11	☐	☐	US 5422582 A	19950606	9	Diode coupled CMOS logic design for quasi-static	326/95	326/136

WEST

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Search Results -

Terms	Documents
L1 and (power same ground)	47

Database:
US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear

Search History

DATE: Monday, December 08, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L2	L1 and (power same ground)	47	L2
L1	5210855.uref.	141	L1

END OF SEARCH HISTORY

WEST

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Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
L2	0

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L3

Refine Search | Recall Text | Clear

Search History

DATE: Monday, December 08, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 and (power same ground)	47	L2
L1	5210855.uref.	141	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L5 and (ground same power)	180

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L6

Refine Search | Recall Text | Clear

Search History

DATE: Monday, December 08, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L6	L5 and (ground same power)	180	L6
L5	((710/301 |710/302)!.CCLS.)	556	L5
L4	(710/301,302.ccls.) and (power same ground)	0	L4
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 and (power same ground)	47	L2
L1	5210855.uref.	141	L1

END OF SEARCH HISTORY

WEST

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Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
L1 and (hot adj1 (plug$5 or swap$5))	80

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L3

Refine Search | Recall Text | Clear

Search History

DATE: Wednesday, December 03, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L3	L1 and (hot adj1 (plug$5 or swap$5))	80	L3
L2	L1 and (hot adj1 (plug$5 or swap$4))	77	L2
L1	ground same power same (switch$4 or isolat$3 or disabl$3)	10094	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L3	0

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear

Search History

DATE: Wednesday, December 03, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT; PLUR=YES; OP=OR			
L3	L1 and (hot adj1 (plug$5 or swap$5))	80	L3
L2	L1 and (hot adj1 (plug$5 or swap$4))	77	L2
L1	ground same power same (switch$3 or isolat$3 or disabl$3)	10094	L1

END OF SEARCH HISTORY

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Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
l3 and ((input adj1 output) or (I adj1 O) or signal)	79

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L5

Refine Search | Recall Text | Clear

Search History

DATE: Wednesday, December 03, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L5	l3 and ((input adj1 output) or (I adj1 O) or signal)	79	L5
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT; PLUR=YES; OP=OR			
L3	L1 and (hot adj1 (plug$5 or swap$5))	80	L3
L2	L1 and (hot adj1 (plug$5 or swap$4))	77	L2
L1	ground same power same (switch$3 or isolat$3 or disabl$3)	10094	L1

END OF SEARCH HISTORY

WEST

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Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
((361/58 |361/686)!.CCLS. |(710/301 |710/302 |710/313)!.CCLS. |(323/908)!.CCLS. |(307/130 |307/11 |307/126)!.CCLS. |(713/300)!.CCLS.)	4053

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear

Search History

DATE: Monday, December 08, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L1	((361/58 |361/686)!.CCLS. |(710/301 |710/302 |710/313)!.CCLS. |(323/908)!.CCLS. |(307/130 |307/11 |307/126)!.CCLS. |(713/300)!.CCLS.)	4053	L1

END OF SEARCH HISTORY

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Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
l1 and L3	6

Database:
US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear

Search History

DATE: Monday, December 08, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L4	l1 and L3	6	L4
L3	L2 and (hot adj1 (plug$5 or swap$5))	24	L3
L2	ground same power same switch$3 same (isolat$3 or disabl$3)	3337	L2
L1	((361/58 |361/686)!.CCLS. |(710/301 |710/302 |710/313)!.CCLS. |(323/908)!.CCLS. |(307/130 |307/11 |307/126)!.CCLS. |(713/300)!.CCLS.)	4053	L1

END OF SEARCH HISTORY

DOCUMENT-IDENTIFIER: US 6542997 B1
TITLE: Powering computer systems

Brief Summary Text (12):
The power sub-system can include a power distribution board with power distribution logic operable to distribute power from the power supply units for powering the processor module, the power distribution circuitry being operable to interrupt power for powering the processor module when two of the power supply units fail or are not present. A plurality of power rails can be provided on the power distribution board to separate power supplies for various system components, thus enhancing noise and signal separation.

Detailed Description Text (14):
FIG. 6 is a rear view of the unit 10 in a configuration with three DC power supply units 74A, 74B and 74C. Each of the power supply units 74A, 74B and 74C is the same, and provides redundant power for the unit 10. However, as will be seen later, one or more of the DC power supply units could be replaced by AC (mains) power supply units. The power supplies are hot swappable (i.e., while the system is running), as long as they are swapped one at a time.

Detailed Description Text (16):
Also shown is a grounding plate 100 that is secured by knurled nuts 102, 104 and 106 to grounding studs 103, 105 and 107. Grounding stud 103 provides a connection directly to the chassis 11 of the unit 10. Grounding studs 105 and 107, on the other hand are electrically isolated from the chassis by an insulating board and are instead connected to logic ground (i.e. the ground of the electronic circuitry). By means of the grounding plate 100, logic ground can be connected directly to chassis ground. The provision of this grounding plate provides for optional tying of logic ground to chassis ground. It will be noted that each of the power supply units 74 is provided with a similar grounding plate 100, for connection to corresponding grounding studs. If it is desired to isolate logic ground from chassis ground, it is necessary to remove the grounding plate 100 from each of the power supply units 74A, 74B and 74C.

Detailed Description Text (17):
An isolated ground system is needed in some telco applications when operating in a Regional Bell Operating Company (RBOC) mode. When operating in such a mode, the chassis and logic ground are connected at a remote location to provide, for example, lightning protection. In this case two-hole lugs 101 having a pair of holes 111 to fit over the pair of grounding studs 105 and 107 are provided for each of the power supply units 74 and are secured over the studs using nuts 104 and 106. A similar two-hole lug 101 is secured to the grounding studs 108 and is secured with similar nuts. Earthing wires 109 from each of the two-hole lugs 101 on the power units and the chassis then are taken to the remote, earthing location. The studs 103105, 107 and 108 are of a standard thread size (M5). The studs 105/107 and the studs 108 are at a standard separation (15.85 mm). The studs 105/107 are self-retaining in the insulated board on the power supply units. The stud 103 is self-retaining in the casing of its power supply unit 74. The suds 108 are also self-retaining in the system unit chassis.

Detailed Description Text (18):
In a non-isolated ground situation, chassis ground can simply be tied to a desired

ground potential (for example, to the racking system) by connecting a grounding cable to grounding studs 108 provided on the rear of the chassis. A further earth connection is provided via the power cables for the power supplies.

Detailed Description Text (21):
FIG. 8 is a schematic overview of the computer architecture of the system 10. As shown in FIG. 8, various components within the system are implemented through application-specific integrated circuits (ASICs). The system is based round a UltraSparc Port Architecture (UPA) bus system that uses a Peripheral Component Interconnect (PCI) protocol for an I/O expansion bus. The CPU modules 40.0, 40.1, 40.2, 40.3, and a UPA-TO-PCI (U2P) ASIC 154 communicate with each other using the UPA protocol. The CPU modules 40 and the U2P ASIC 154 are configured as UPA master-slave devices. An Address Router (AR) ASIC 154 routes UPA request packets through the UPA address bus and controls the flow of data to and from memory 150 using a Data Router (DR) ASIC 144 and a switching network 148. The AR ASIC 154 provides system control. It controls the UPA interconnect between the major system components and main memory.

Detailed Description Text (22):
The DR ASIC 144 is a buffered memory crossbar device that acts as a bridge between six system unit buses. The six system unit buses include two processor buses, a memory data bus and to I/O buses. The DR ASIC 144 provides crossbar functions, memory port decoupling, burst transfer and First-in-First-Out (FIFO) data read functions. Clock control for the operation of the processor is provided by a Reset, Interrupt, Scan and Clock (RISC) ASIC 152.

Detailed Description Text (23):
The PCI bus is a high performance 32-bit or 64-bit bus with multiplexed address and data lines. The PCI bus provides electrical interconnection between highly integrated peripheral controller components, peripheral add-on devices, and the processor-memory system. A one-slot PCI bus 155 connects to a PCI device 156.0. A three-slot PCI bus connects to three PCI slots 156.1, 156.2 and 156.3. Two controllers are also connected to the second PCI bus 157. These include a SCSI controller 174 and a PCI-TO-EBus/Ethernet controller (PCIO) 158. The SCSI controller 174 provides electrical connection between the motherboard and separate internal and external SCSI buses. The controller also provides for SCSI bus control. The PCIO 158 connects the PCI bus to the EBus. This enables communication between the PCI bus and all miscellaneous I/O functions as well as the connection to slower, on board functions. Thus, the PCIO enables the connection to an Ethernet connection via a Transmit/Receive (Tx/Rx) module 161 and a network device (ND) module 162.

Detailed Description Text (24):
An EBus2159 provides a connection to various I/O devices and internal components. Super I/O 164 is a commercial off-the-shelf component that contains two serial port controllers for keyboard and mouse, an IEEE 1284 parallel port interface and an IDE disk interface. The super I/O drives the various ports directly with some electromagnetic interference filtering on the keyboard and parallel port signals. The alarms module 78 interfaces with the motherboard and provides various alarm functions. The NVRAM/TOD 168 provides non-volatile read only memory and the time of day function. Serial port 170 provides a variety of functions. Modem connection to the serial port 170 enables access to the Internet. Synchronous X.25 modems can be used for telecommunications in Europe. An ASCII text window is accessible through the serial port on non-graphics systems. Low speed printers, button boxes (for computer aided design applications) and devices that function like a mouse are also accessible through the serial port. The serial port includes a serial port controller, line drivers and line receivers. A one-Mbyte flash programmable read only memory (PROM) 172 provides read only memory for the system.

Detailed Description Text (25):
FIG. 9 is a perspective rear view of the system 10 showing the withdrawal and/or insertion of a power supply unit 74 in a non-isolated ground situation. In this example, AC power supply units 74 are shown. It can be seen that the power supply unit 74 is provided with the handle 94. As shown in FIG. 9, the handle 94 is provided with a grip 184, a pivot 182 and a latch 180. To insert the power supply unit 74 it is necessary to slide the power supply unit into the power sub-frame 72

with the grip 184 of the handle 94 slightly raised so that the detent 180 can be received under the top 184 of the power sub-frame 72. As the power supply unit 74 reaches the end of its movement into the power sub-frame 72, connectors (not shown) provided on the power supply unit 74 make connection with a corresponding connector on the power distribution board at the rear of the power sub-frame 72. Also, at this time, the handle can be pushed down into the position shown in FIG. 9. This causes the detent 180 to latch behind the upper portion 184 of the power sub-frame 72. The handle 94 can then be secured in place by tightening the screw 95. The AC power supply unit 74 shown in FIG. 9 has a single power socket 97, whereas the DC power supply units 74 shown in FIG. 6 have two power sockets 96 and 98. Irrespective of whether the arrangement is as shown in FIG. 6 with two DC power sockets 96 and 98, or as shown in FIG. 9 with one AC power socket 97, the configuration of the power socket(s) and the lever 94 is such that the lever cannot be moved, and therefore the power supply unit cannot be released from the power sub-frame 72 and the chassis 11 with a plug 186 of a power cable 188 in place in one of the power sockets 96/97/98. The removal operation is achieved by releasing the screw 95, removing the power plug, and lifting and pulling on the handle 94.

Detailed Description Text (26):
In an isolated ground situation, in order to hot-swap a power supply unit 74, it is merely necessary to remove the two-hole lug 101 with its connecting earth wire 109 from the studs 105, 107 of the power supply unit to be removed, to remove the old power supply unit 74, to replace a new power supply unit 74 and then to reconnect the two-hole lug 101 and connecting earth wire 109 to the studs 105, 107 of the new power supply unit 74. These operations can all be performed with the system under power from the other power supply units 74 and with the two-hole lugs 101 and earth wires 109 in place over the chassis studs 108 and the studs 105, 107 of the other power supply units 74.

Detailed Description Text (27):
The isolated ground situation is not shown in FIGS. 6 and 9. In the non-isolated ground situation shown in FIGS. 6 and 9, hot-swapping of a power supply unit is even easier, as it is merely necessary to remove the selected power supply unit 74 and to replace it with the new power supply unit 74.

Detailed Description Text (32):
FIG. 10C shows the open (front) side 195 (see FIG. 10B) of the power sub-frame. When inserted in the chassis of the system unit, this "front" of the power sub-frame is actually the rear-most side of the power sub-frame when viewed with respect to the system unit. Within the power sub-frame 72, connectors 192A, 192B and 192C for the three power supply units 74A, 74B and 74C, respectively, can be seen. These connectors are mounted on the power distribution board 190 inside the power sub-frame 72. FIG. 10C also shows the flanges 198 with screw holes 199 for securing the power sub-frame to the rear chassis wall. FIG. 10D is a perspective view of the power sub-frame 72, which shows that this in fact forms part of a power sub-assembly 71. Internal walls 200 separate three compartments, each for a respective one of the three power supply units 74. Cables 202 connect standby power and signal lines from the power distribution board 190 to a connector 204 for connection to an alarms module. Cables 206 connect main power and signal lines from the power distribution board 190 to various connectors 208, 210, 212 and 214. FIG. 10E shows the various connector types 192, 204, 208, 210, 212 and 214 and the electrical signal connections thereto.

Detailed Description Text (34):
At the left of FIG. 11, the three connectors 192A, 192B and 192C for the three power supply units 74A, 74B and 74C are shown. For reasons of clarity and convenience only those connections relevant for an understanding of the present invention as shown. For example, as illustrated with respect to FIG. 10E, the connectors 192 have many pins and pass many signals via respective lines. However, as not all of these lines are necessary for an understanding of the present invention, and as it would be confusing to illustrate all of the signal pathways on a diagram, only selected pathways are shown in FIG. 11. It is to be noted from FIG. 10E, that the power supply units output ground, +3V3, +5V, +12V, -12V and +5V standby potentials as well as control signals such as PSU OK, PSU ON, etc. The +5V standby voltage is used for powering the alarm module 78. The other voltages are for powering the motherboard

and other main system components. The various lines could be configured using bus bars, wires, printed circuit or thick film conductors as appropriate.

Detailed Description Text (35):
Firstly, the two-of-three circuit 232 will be explained. This circuit is powered by the +5V standby voltage 231 provided from each of the power supply units 74. Each of the power supply units outputs a PSU OK signal via a pin on its respective connector to a corresponding PSU OK line 230A, 230B and 230C when the power supply unit is operating correctly. Each of these PSU OK lines 230 is connected to the two-of-three circuit 232. This comprises three AND gates 234, 236 and 238,

Detailed Description Text (36):
each for comparing a respective pair of the PSU OK signals. The outputs of the AND gates are supplied to an OR gate 240.

Detailed Description Text (37):
If the output of this OR gate is true, then at least two of the power supply units 74 are operating correctly, and power can be supplied to the motherboard of the computer system. This can be achieved by closing the main power line 245. An output signal 242 could be supplied to a gate 244 (for example a power FET) to enable current to pass to the motherboard and other system components.

Detailed Description Text (38):
Additionally, or alternatively, a power OK signal 246 for controlling some other form of switch mechanism (not shown).

Detailed Description Text (39):
If alternatively the output of the OR gate 242 is false, then this indicates less than two of the power supply units 74 are operative. In this case power is prevented from being passed to the motherboard 40 of the computer system. This can be achieved by interrupting the main power line 245. An output signal 242 could be supplied to a gate 244 (for example a power FET) to prevent current being passed to the motherboard and other system components. Additionally, or alternatively, a power fault signal 246 could be passed to the alarms module and/or for controlling some other form of switch mechanism (not shown).

Detailed Description Text (40):
One-of-three power control is effectively provided by the alarms module 78 to be described later. However, with reference to FIG. 11, input A/B signals 268 and output sense signals 270 are passed to the alarms module for standby operation, and control signals 272 could be returned for turning off of a power supply unit, if required.

Detailed Description Text (42):
Thus, as shown in FIG. 11, each of the main power lines (e.g., +12V) 250A, 250B and 250C from the power supply units 74A, 74B and 74C, respectively is connected to form a common power supply line 254. An overcurrent detector 258 detects a current in excess of 2*Imax. If such a current is detected (for example as a result of a fault represented by the box 266), then a signal 261 is provided to the connectors 192,A, 192B and 192C for shutting down the power supplies 74A, 74B and 74C, respectively. Also, a signal 262 is passed to a switchable shunt 260 (e.g., a silicon controlled rectifier (SCR), a Metal Oxide Semiconductor Field Effect Transistor (MOSFET), an Insulated Gate Bipolar Transistor (IGBP), etc) to shunt the power supply line 254 to ground. This will cause any energy stored in the power supplies and also in the system (for example as represented by the capacitor 264) to drain to ground, thus protecting the system.

Detailed Description Text (43):
The use of the two-of-three circuit described above means that redundant power supply operation is provided in that the system can remain powered even if one of the three power supply units fails. As only two-of-three power supply units are needed to power the system the third power supply unit can be hot swapped while the other two power supply units power the system.

Detailed Description Text (46):

The alarms sub-system comprises a logic device 280 which receives inputs 298 from the EBus, inputs 286 from the fans, input 290 from general purpose events, input 270 from the power supply unit output rails and inputs 268 from the A and B power inlets. The logic circuit samples, or multiplexes, the inputs to the microcontroller 296 in response to multiplex signals from the microcontroller 296. The microcontroller 296 processes the sampled (multiplexed) inputs. The microcontroller 296 provides power control signals 272 for controlling the power supply units, and alarm outputs for the output of alarm signals. The microcontroller 296 also outputs power supply unit status signals 304 and fault signals 306. The micro controller 296 can further output a system reset signal 310, when required. Alarm signals to be passed to a remote location can pass via a remote serial connection 112. Diagnostic and remote control signals can be passed from the network via the serial connection 112 to the microcontroller 296. Control signals can thus be provided via the remote serial connection over the network for powering on and powering off the system. Examples of other commands that can be sent to the microcontroller via the remote serial connection 112 are to turn alarms off, to reset the monitoring of all failures, to display the status of all fans, power supply units, alarms and fault Light Emitting Diodes (LEDs), to display an event log, etc.

Detailed Description Text (49):
For convenience, tacho (speed) signals from the fans pass via the alarms control module 66. The speed signals are not processed by the fan control module, but are instead forwarded via tacho sense 326 to the power distribution board 190. The power distribution board then routes the tacho sense signals to the alarms module 78 to form the signals 286 shown in FIG. 13. This routing is convenient as it enables simpler wiring looms to be used. Also, when replacing a fan unit, the maintenance engineer only needs to remove a single bundle of wires from the fan to the fan control module 66, rather than having to locate a number of different connectors connected to the fan. The fan control module thus has four fan connectors, each for receiving a connector connected to a bundle of wiring from a respective fan, plus a further connector for receiving a connector with a bundle of wires from the power distribution board.

Detailed Description Text (50):
As shown in FIG. 14, each half 66A/66B of the fan control module receives respective power lines 324A/B from the power distribution board. Each half of the fan control module includes electrical noise isolation circuitry 340A/B. This electrical noise isolation circuitry 325 A/B, which can be of conventional construction, prevents dirty power signals on the lines 320A/B caused by electrical noise from the fans being passed back along the power lines 324A/B and potentially contaminating the otherwise clean power supply to the electronics of the system unit (e.g., the components on the SCSI bus. The provision of clean power supply signals in a telco application is important in order to ensure reliability of operation. Although in the present example the noise isolation circuitry is located in the fan control module, it could be located elsewhere as long as it is effective to isolate the main power lines from fan-related electrical noise.

Detailed Description Text (51):
As further shown in FIG. 14, each side 66A/B of the fan control module comprises control logic 342A/B which receives a temperature signal from a temperature sensor 344 and adjusts the speed of the fans by adjusting the voltage supplied thereto in accordance with pre-programmed parameters in order to provide a desired degree of cooling. The control logic 342A/B can be implemented by an ASIC, a programmable logic array, or any other appropriate programmable logic. Alternatively, it could be implemented by software running on a microcontroller or microprocessor module.

Detailed Description Text (52):
It should be noted that the fan control module could be implemented in a unitary manner, rather than being divided into two halves. Although in the present instance the fan control module is preferably configured on a single circuit board, this need not be the case. Also, although the temperature sensor is also mounted on the same circuit board, it could be mounted elsewhere. Moreover, although it is preferred that a single temperature sensor is used, with the advantage that the fan speeds of the respective fans can be ramped up in parallel in a controlled manner, more than one temperature sensor could be used. Ideally, in this case they would be located

close together and control of the individual fans could be dependent on individual signals but would more preferably be dependent on a function of some or all of the temperature signals. As a further feature, the control logic could be provided with different sets of programmed parameters depending on the number of processors present and could be responsive to the number of processors present.

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L5: Entry 10 of 79 File: USPT Apr 1, 2003

US-PAT-NO: 6542997
DOCUMENT-IDENTIFIER: US 6542997 B1

TITLE: Powering computer systems

DATE-ISSUED: April 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rolls; Jeremy B.	Wimbledon			GB
Bushue; Michael J.	Belmont	CA		
Rumney; Gary S.	Leighton Buzzard			GB
Jones; Rhod J.	Crowthorne			GB
Liddell; David C.	Gosforth			GB
Heffernan; Peter	Chandlers Ford			GB

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Santa Clara	CA			02

APPL-NO: 09/ 415766 [PALM]
DATE FILED: October 8, 1999

INT-CL: [07] G06 F 1/26, G06 F 1/28, G06 F 1/30

US-CL-ISSUED: 713/324; 713/300, 713/320, 713/324, 713/340
US-CL-CURRENT: 713/324; 713/300, 713/320, 713/340

FIELD-OF-SEARCH: 713/324, 713/340, 713/320, 713/300, 363/65, 361/683, 307/64

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3983554	September 1976	Goode	340/502
☐	4698738	October 1987	Miller et al.	363/65
☐	4729086	March 1988	Lethellier	307/53
☐	5726866	March 1998	Allen	361/683
☐	6233692	May 2001	Villanueva	709/217

ART-UNIT: 2185

PRIMARY-EXAMINER: Lee; Thomas

ASSISTANT-EXAMINER: Nguyen; Thong-Thai T

ATTY-AGENT-FIRM: Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Kivlin; B. Noel

ABSTRACT:

A computer system includes a chassis with a single motherboard supporting at least one processor module. A power sub-system receives three power supply units and distributes power within the computer system. Each of the three power supplies has a power rating such that two of the three power supplies are sufficient to power the computer system. The combination of such a single-motherboard-based design with a redundant three-power supply sub-system provides reliability of operation in a cost-effective manner. The power sub-system includes a power distribution board with power distribution logic operable to distribute power from the power supply units for powering the processor module. The power distribution logic is operable to interrupt power for powering the processor module when two of the power supply units fail or are not present. An alarm sub-system is provided for reporting power supply faults.

17 Claims, 20 Drawing figures

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L5: Entry 19 of 79 File: USPT Sep 17, 2002

US-PAT-NO: 6452794
DOCUMENT-IDENTIFIER: US 6452794 B1
**** See image for Certificate of Correction ****

TITLE: Grounding computer systems

DATE-ISSUED: September 17, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rumney; Gary S.	Leighton Buzzard			GB

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Palo Alto	CA			02

APPL-NO: 09/ 415110 [PALM]
DATE FILED: October 8, 1999

INT-CL: [07] G06 F 1/16

US-CL-ISSUED: 361/686; 361/753, 323/259
US-CL-CURRENT: 361/686; 323/259, 361/753

FIELD-OF-SEARCH: 361/679, 361/753, 361/799, 361/784, 361/785, 361/794, 361/795, 361/686, 174/51, 307/150, 333/104, 333/116, 333/123, 333/124, 333/160, 333/161, 333/206, 333/238, 333/247, 333/246, 439/63, 439/578, 439/581, 439/607, 439/608, 439/944, 364/240, 364/240.1-240.7, 323/259

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5689180	November 1997	Carlson	323/359
☐	5971804	October 1999	Gallagher et al.	439/581

ART-UNIT: 2835

PRIMARY-EXAMINER: Schuberg; Darren

ASSISTANT-EXAMINER: Chang; Yean-Hsi

ATTY-AGENT-FIRM: Conley, Rose & Tayon, PC Kivlin; B. Noel

ABSTRACT:

A computer system includes a chassis, electronic circuitry, a plurality of removable power supply units, and a power distribution mechanism to which the power supply units are connectable. The chassis includes at least one connector for effecting a connection to a first, chassis, ground potential. The electrical circuitry is connected to a second, logic, ground potential. Each of the power supply units is provided with a separate removable grounding plate for selectively coupling chassis ground to logic ground. The use of a power distribution mechanism with a plurality of removable power supply units enables redundancy for the power supply units, whereby the system can remain powered when one of the power supply units fail. The use of the grounding plates for each of the power supply units enables reliable connection of the electrical and chassis grounds can be effected, even when one of the power supply units and/or its connecting cable is faulty. When it is desired to isolate the electrical and chassis grounds, then all of the grounding plates can be removed.

33 Claims, 20 Drawing figures

L5: Entry 21 of 79 File: USPT Jun 18, 2002

DOCUMENT-IDENTIFIER: US 6408343 B1
TITLE: Apparatus and method for failover detection

Abstract Text (1):
A device and method for a peripheral adapter of a dual SCSI bus enclosure is described. An adapter can operate alone or in pairs to provide different modes of operation, including simplex, duplex, and cluster. When used in pairs, two adapters interconnect internally to the enclosure through internal cross-coupling bus repeaters that can be selectively enabled or disabled. The adapters are hot-swappable and have the ability to automatically self configure. In the cluster mode, the adapter supports failover capability from a master adapter to a redundant adapter.

Brief Summary Text (4):
SCSI (small computer systems interface) is a commonly used parallel I/O (input/output) system for computers. Computers can be interconnected with peripherals or modules along a SCSI bus or SCSI channel. A common interconnection arrangement is a daisy chain, where the bus extends out of one module into the next peripheral. The number of modules on a SCSI channel is bound by a fixed upper limit (e.g., 8 or 16, including the host computer). Although ANSI (American National Standards Institute) standards documents exist for SCSI, many variations are possible and proprietary adaptations are common. For example, a SCSI-1 bus is a 50 conductor, single ended, parallel bus; a SCSI-2 bus is an extension of SCSI-1 to 68 conductors; and SCSI-3 is a faster, low voltage differential version of SCSI-2. SCSI requires termination at the ends of the bus, and the terminations may be either active or passive and may be either internal or external to the peripheral. Finally, a variety of SCSI connectors can be used.

Brief Summary Text (5):
FIG. 1 illustrates a computer system and various peripheral devices interconnected by a single SCSI I/O bus. A computer 100 includes two internal SCSI devices 102 and 104. The internal devices 102 and 104 might be, for example, a disk drive and a backup tape drive. Two external devices 106 and 108 are also connected to the SCSI bus. The external SCSI devices might be, for example, a printer and a scanner. In general, the SCSI bus system may have more or fewer devices. In the SCSI system illustrated in FIG. 1, the internal device 102 must provide a bus termination impedance. The internal devices 102 and 104 are typically connected by a ribbon cable with a single connector (for example, 110) for each device. The external devices 106 and 108 are typically connected by a series of double ended cables. A first cable connects a connector 112 on the computer 100 to the external device 106. A second cable connects the external device 106 to the external device 108. The external device 108 has an open connector 114 (no cable attached) that may be terminated with an external terminator plug 116 (mandatory for Plug and Play SCSI) or may be terminated internally to the device 108. The total length of a SCSI bus to a final termination must be less than a predetermined limit so as to ensure signal integrity along the entire bus.

Brief Summary Text (17):
The configurations of FIGS. 2-4 illustrate several problems that the present invention is capable of solving. First, there is wasteful redundancy of processing capability and SCSI addressing space. The adapter board 250 contains two active SEPs, regardless of whether both are needed. Only the duplex configuration of FIG. 3

requires that the SEPs 252 and 254 operate independently. In the other configurations, the second SEP 254 is not utilized to enhance the availability, fault-tolerance, or robustness of the enclosure processing capability. In particular, failover from an active SEP to a standby SEP is not possible. Furthermore, the second SEP 254 occupies one SCSI address that is therefore unavailable for use by a productive module or peripheral. A second problem is that hot-swapping of an SEP is not possible, because both SEPs are physically mounted on the same board. Instead, operation of the system must be halted in order to remove and replace an SEP or adapter board. A third problem is that setting up the adapter board 250 in different configurations requires operator intervention and external SCSI bus jumpers, which disadvantageously add to the total bus length. A fourth problem occurs in the cluster configuration of FIG. 4 when either the jumper cable 302 or one of the computers 300 or 306 becomes disconnected, resulting in an end of the bus, as seen by the remaining computer, being unterminated and therefore unusable. The present invention can be utilized to solve these and other problems.

Brief Summary Text (19):
The present invention is a device and method for a peripheral adapter that can be efficiently configured to different modes of operation, including simplex, duplex, and cluster. In one form, the present invention is an adapter containing master components and/or redundant components. The adapter can be utilized in an enclosure alone or in pairs. In pairs, the adapters interconnect internally to the enclosure through internal bus repeaters. The adapter(s) automatically self configure and are hot-swappable. In the cluster mode, failover from a master adapter to a redundant adapter is possible. The present invention provides an adapter that is modular, flexible, and offers higher availability, fault-tolerance, and robustness with a minimum of operator intervention.

Detailed Description Text (3):
In FIG. 5, the enclosure 400 is attachable to the outside world through an adapter 450 at a single external host connector 451. The adapter 450 contains a single SEP 452 and two peripheral connectors 453 and 455 that are internal to the enclosure, linking the adapter 450 to the two SCSI buses 420 and 440, respectively. All connectors (451, 453, and 455) support hot plug-in and unplugging (i.e., engagement and disengagement to/from the connectors while power is applied), according to well known practices in the art. The adapter 450 also contains two SCSI repeators--a host or external connection repeater 456 near the external host connector 451 and a peripheral or internal cross-coupling repeater 459 near the internal peripheral connector 455. The internal peripheral connectors 453 and 455 are linked to the other components of the adapter 450. For instance, the internal peripheral connector 453 is linked to the SEP 452 and the external host repeater 456 by direct electrical connections. The internal peripheral connector 455 is linked to the same other components through the cross coupling repeater 459, which may be enabled or disabled. We say that the cross coupling repeater 459 provides a link even when the repeater is disabled, because a connection can always be realized by simply enabling the repeater 459. Depending upon whether a second adapter is present in the enclosure 400 and the settings of the adapters' repeaters and SEPs, the two SCSI bus systems of enclosure 400 can be utilized in a simplex, duplex, or cluster configuration, as will next be described.

Detailed Description Text (10):
Another mechanism for detecting failure is receipt of an interrupt signal by the second SEP 472. The interrupt may originate from any source, including the first SEP 452, the host computer 300 or 306, or other hardware. In response to the interrupt signal, the second SEP 472 initiates processing to assume active status with the identity of the failed first SEP 452. Programing instructions that perform this processing may be stored as an interrupt procedure in memory associated with the second SEP 452. The memory may be internal to the second SEP 452 or external (not shown in the figures).

Detailed Description Text (11):
Failure detection by receipt of an interrupt signal and failure detection by a periodic communications scheme may operate together. The same interrupt procedure can perform processing in response to either detection mechanism. In the case of failure detection by receipt of an interrupt signal, the call to the interrupt

procedure is hardware generated. In the case of failure detection by a periodic communications scheme, the call to the interrupt procedure is software generated. Other mechanisms for failure detection may be likewise combined in concert.

Detailed Description Text (12):
The fail over capability enables hot-swapping of a master adapter. Hot-swapping is removal and insertion of computer hardware without powering down the computer hardware or associated equipment. Hot-swapping allows computer equipment to be repaired, tested in isolation, and upgraded without disabling operation of the system and thereby decreasing availability. Hot-swapping of a critical piece of equipment is possible only when the system provides separable redundancy in that equipment. In addition, the equipment must be designed with the physically capability of removal and insertion while power is applied, according to well known practices in the art (e.g., connection of ground conductors, power conductor, then signal conductors in that order). Further, some mechanism for activity transition between redundant units during hot-swapping must be provided. The failover process of the present invention serves this purpose.

Detailed Description Text (13):
Failover, as described above, allows hot-swapping of the first adapter 450. Removal of the first adapter 450 causes a failure of the first SEP 452. This failure may manifest itself as loss of communication in a periodic ping scheme, or removal may trigger a SCSI reset signal that can be hardwired into an interrupt input of the second SEP 472. Generation of a suitable SCSI reset signal is described in commonly assigned patent application Ser. No. 09/272,798, entitled "State Activating One Shot with Extended Pulse Timing for Hot-Swap Applications," and hereby incorporated by reference. Alternatively, removal may trigger an analog hardwired signal. In any case, the second SEP 472 detects the failure and activates itself while performing other necessary adjustments to the adapter 470, such as enabling the internal cross-coupling repeater 479. Insertion of the first adapter 450 back into the enclosure 404 causes the first adapter 450 to self configure (as described below), which would result in disabling cross-coupling repeater 459 and setting SEP 452 into a standby mode.

Detailed Description Text (14):
Self configuration also allows hot-swapping of an adapter in the standby state. Consider, for example, hot-swapping of the adapter 470 in the initial configuration of FIG. 7. In that case, SEP failover is not necessary. The adapter 470 is simply removed, and, after reinsertion, it automatically configures itself back into the same condition by enabling the external connection repeater 476, disabling the internal cross-coupling repeater 479 and setting the SEP 472 into a standby mode.

Detailed Description Text (15):
Automatic configuration of the first adapter 450, for example, is possible with knowledge of (1) whether the second adapter 470 is plugged in the enclosure 404 and (2) whether clustering is enabled or disabled. The presence of the second adapter 470 in the enclosure 404 may be sensed in any number of ways within the skill of an ordinary engineer in the art. For instance, presence of a second adapter in the enclosure can close a simple conduction pathway to create a signal line to the first adapter. Clustering can be enabled or disabled by a mechanical switch setting, such as a DIP (dual in-line package) switch, on the adapter 450. Alternatively, SCSI commands or host computer commands can communicate these two pieces of information to the adapter 450.

CLAIMS:

8. The adapter of claim 3 wherein the adapter is hot-swappable.

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L5: Entry 21 of 79 File: USPT Jun 18, 2002

US-PAT-NO: 6408343
DOCUMENT-IDENTIFIER: US 6408343 B1

TITLE: Apparatus and method for failover detection

DATE-ISSUED: June 18, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Erickson; Michael J.	Loveland	CO		
Zilavy; Daniel V.	Ft. Collins	CO		
Strunk; Glenn W.	Ft. Collins	CO		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

APPL-NO: 09/ 274385 [PALM]
DATE FILED: March 29, 1999

INT-CL: [07] G06 F 13/14, G06 F 13/20

US-CL-ISSUED: 710/15; 710/18, 714/11, 714/25, 714/40, 714/44
US-CL-CURRENT: 710/15; 710/18, 714/11, 714/25, 714/40, 714/44

FIELD-OF-SEARCH: 710/15, 710/18, 714/44, 714/40, 714/25, 714/11

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5574726	November 1996	Chan et al.	370/85.3
☐	5586250	December 1996	Carbonneau et al.	395/183.2
☐	6003075	December 1999	Arendt et al.	709/221
☐	H1882	October 2000	Asthana et al.	370/503

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IBM TDB, `Fault Telerant Architecture for Communication Adapters and Systems`, vol. 35, Issue 7, pp. 300-303, Dec./1992.*
IBM TDB, `Keep Alive Redundancy and Back-Up for T3 and E3/E2/J2 Lines`, vol. 38, Issue 1, pp. 551-552, Jan.-1995.

ART-UNIT: 2182

PRIMARY-EXAMINER: Gaffin; Jeffrey

ASSISTANT-EXAMINER: Perveen; Rehana

ABSTRACT:

A device and method for a peripheral adapter of a dual SCSI bus enclosure is described. An adapter can operate alone or in pairs to provide different modes of operation, including simplex, duplex, and cluster. When used in pairs, two adapters interconnect internally to the enclosure through internal cross-coupling bus repeaters that can be selectively enabled or disabled. The adapters are hot-swappable and have the ability to automatically self configure. In the cluster mode, the adapter supports failover capability from a master adapter to a redundant adapter.

18 Claims, 9 Drawing figures

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L9: Entry 1 of 6 File: USPT Jul 1, 2003

DOCUMENT-IDENTIFIER: US 6587908 B2
TITLE: Processor design with improved condition sensing

Abstract Text (1):
An invention is disclosed for providing a signal indicating whether a processor is installed and providing improved voltage regulation. A contact is selected and isolated from an array of ground contacts and is further coupled with circuit for generating an INSTALL signal. A capacitor and pull up resistor coupled to a supply voltage, ground and the isolated contact form a signal line at a common node such that a circuit to ground is completed through the processor and the isolated contact when the processor is plugged in and a direct signal indication of the presence or absence of the processor is provided. Voltage sense lines of a Voltage Regulation Module (VRM) are coupled directly to processor contacts isolated from an existing voltage supply contacts coupled to the supply plane of a supply voltage within the circuit board providing improved regulation without adversely affecting power supply current capacity considerations.

Current US Cross Reference Classification (4):
710/301

WEST

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L9: Entry 1 of 6 File: USPT Jul 1, 2003

US-PAT-NO: 6587908
DOCUMENT-IDENTIFIER: US 6587908 B2

TITLE: Processor design with improved condition sensing

DATE-ISSUED: July 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sanders; Michael C.	Spring	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Development Company, L.P.	Houston	TX			02

APPL-NO: 10/ 224842 [PALM]
DATE FILED: August 21, 2002

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This application is a continuation of U.S. application Ser. No. 09/881,423, filed Jun. 14, 2001, now U.S. Pat. No. 6,502,153, issued on Dec. 31, 2002, which is a continuation of U.S. application Ser. No. 09/249,184, filed Feb. 12, 1999, now U.S. Pat. No. 6,263,386, issued Jul. 17, 2001.

INT-CL: [07] G06 F 13/00, H05 K 7/10

US-CL-ISSUED: 710/300; 710/301, 361/785, 361/809, 439/55
US-CL-CURRENT: 710/300; 361/785, 361/809, 439/55, 710/301

FIELD-OF-SEARCH: 710/300-302, 712/32, 361/763, 361/764, 361/748, 361/736, 361/794, 361/785, 361/807, 361/809, 257/734, 257/700, 333/247, 713/300, 439/101, 439/55, 439/68, 439/75

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4084869	April 1978	Yen	339/17CF
☐	5244397	September 1993	Anhalt	
☐	5384692	January 1995	Jaff	361/807
☐	5432505	July 1995	Wise	
☐	5442520	August 1995	Kemp et al.	361/785
☐	5587887	December 1996	Price et al.	
☐	5590363	December 1996	Lunsford et al.	395/800
☐	5779502	July 1998	Daftari et al.	439/620
☐	5825630	October 1998	Taylor et al.	360/790
☐	5832294	November 1998	Reinschmidt	395/800.32
☐	6084779	July 2000	Fang	
☐	6108731	August 2000	Suzuki et al.	710/102
☐	6150895	November 2000	Steigerwald et al.	
☐	6359341	March 2002	Huang et al.	

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ABSTRACT:

An invention is disclosed for providing a signal indicating whether a processor is installed and providing improved voltage regulation. A contact is selected and isolated from an array of ground contacts and is further coupled with circuit for generating an INSTALL signal. A capacitor and pull up resistor coupled to a supply voltage, ground and the isolated contact form a signal line at a common node such that a circuit to ground is completed through the processor and the isolated contact when the processor is plugged in and a direct signal indication of the presence or absence of the processor is provided. Voltage sense lines of a Voltage Regulation Module (VRM) are coupled directly to processor contacts isolated from an existing voltage supply contacts coupled to the supply plane of a supply voltage within the circuit board providing improved regulation without adversely affecting power supply current capacity considerations.

22 Claims, 5 Drawing figures

L9: Entry 5 of 6 File: USPT Mar 23, 1999

DOCUMENT-IDENTIFIER: US 5886431 A
TITLE: Circuit and method of operation to control in-rush current from a power supply to peripheral devices in an information system

Abstract Text (1):
This apparatus and method controls and limits the flow of in-rush current to a peripheral device coupled to a main power supply unit through a power bus and a ground bus. The apparatus and method essentially isolate and limit in-rush current flow to a capacitive load until operational current flow occurs to the peripheral device. A switching device is coupled to the power bus and the ground bus through a load. A resistive device is coupled to the power bus and the ground bus through the load. A control circuit is connected to the switching device. During initial start-up or "hot plugging" of the device, the control circuit turns "off" the switching device causing the load to be charged from the power bus through the resistive device until a predetermined condition occurs whereupon the switching circuit is turned "on" to bypass the resistive device and connect the load and the peripheral device to the power bus. Optionally, a uni-directional device may be connected between the power bus and the load to serve as a fail-charge/discharge path to the device in the event the switching device and/or the control circuit should fail. The apparatus and method provide current limiting at power up without requiring the switching component to handle all operational current at all times. Further the apparatus and method allow operation of the device should the switching and/or the control circuit fail.

Current US Cross Reference Classification (4):
710/302

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L9: Entry 5 of 6 File: USPT Mar 23, 1999

US-PAT-NO: 5886431
DOCUMENT-IDENTIFIER: US 5886431 A

TITLE: Circuit and method of operation to control in-rush current from a power supply to peripheral devices in an information system

DATE-ISSUED: March 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rutigliano; Jeffrey Paul	Raleigh	NC		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 08/ 935781 [PALM]
DATE FILED: September 23, 1997

INT-CL: [06] H02 H 9/02

US-CL-ISSUED: 307/131; 323/908, 361/58, 395/283, 439/924.1
US-CL-CURRENT: 307/131; 323/908, 361/58, 439/924.1, 710/302

FIELD-OF-SEARCH: 307/119, 307/116, 307/146, 307/131, 361/58, 361/9, 395/283, 323/908, 439/924.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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☐	5087871	February 1992	Losel	323/908
☐	5187653	February 1993	Lorenz	363/89
☐	5210855	May 1993	Bartol	395/500
☐	5268592	December 1993	Bellamy et al.	307/43
☐	5272584	December 1993	Austruy et al.	361/58
☐	5376831	December 1994	Chen	327/379
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☐	5473499	December 1995	Weir	361/58
☐	5572395	November 1996	Rasums et al.	361/9
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IBM Technical Disclosure Bulletin, vol.34, No. 8, Jan. 1992, pp.52-54, entitled "Power supply Inrush Current-Limiting Circuit".
IBM Technical Disclosure Bulletin, vol. 36, No. 10, Oct. 1993, pp.335-340, entitled "Secondary Power Distribution Source for Point-of Sale Systems".
IBM Technical Disclosure Bulletin, vol. 32, No. 9B, Feb. 1990, pp.424-429, entitled "Hot-Plug Protection Circuit".
IBM Technical Disclosure Bulletin, vol. 24, No. 3, Aug. 1981, pp.1441-1442, entitled "Buck Converter with Switch Referenced to Ground".
IBM Technical Disclosure Bulletin, vol. 25, No. 2, Jul. 1982, p.470, entitled "Power Supply Inrush Current Limiter/Clamp Circuit".

ART-UNIT: 286

PRIMARY-EXAMINER: Paladini; Albert W.

ATTY-AGENT-FIRM: Flynn; John D. Morgan & Finnegan

ABSTRACT:

This apparatus and method controls and limits the flow of in-rush current to a peripheral device coupled to a main power supply unit through a power bus and a ground bus. The apparatus and method essentially isolate and limit in-rush current flow to a capacitive load until operational current flow occurs to the peripheral device. A switching device is coupled to the power bus and the ground bus through a load. A resistive device is coupled to the power bus and the ground bus through the load. A control circuit is connected to the switching device. During initial start-up or "hot plugging" of the device, the control circuit turns "off" the switching device causing the load to be charged from the power bus through the resistive device until a predetermined condition occurs whereupon the switching circuit is turned "on" to bypass the resistive device and connect the load and the peripheral device to the power bus. Optionally, a uni-directional device may be connected between the power bus and the load to serve as a fail-charge/discharge path to the device in the event the switching device and/or the control circuit should fail. The apparatus and method provide current limiting at power up without requiring the switching component to handle all operational current at all times. Further the apparatus and method allow operation of the device should the switching and/or the control circuit fail.

9 Claims, 3 Drawing figures

US-PAT-NO: 5886431

DOCUMENT-IDENTIFIER: US 5886431 A

TITLE: Circuit and method of operation to control in-rush current from a power supply to peripheral devices in an information system

---------- KWIC ---------

Abstract Text - ABTX (1):

This apparatus and method controls and limits the flow of in-rush current to a peripheral device coupled to a main power supply unit through a power bus and a ground bus. The apparatus and method essentially isolate and limit in-rush current flow to a capacitive load until operational current flow occurs to the peripheral device. A switching device is coupled to the power bus and the ground bus through a load. A resistive device is coupled to the power bus and the ground bus through the load. A control circuit is connected to the switching device. During initial start-up or "hot plugging" of the device, the control circuit turns "off" the switching device causing the load to be charged from the power bus through the resistive device until a predetermined condition occurs whereupon the switching circuit is turned "on" to bypass the resistive device and connect the load and the peripheral device to the power bus. Optionally, a uni-directional device may be connected between the power bus and the load to serve as a fail-charge/discharge path to the device in the event the switching device and/or the control circuit should fail. The apparatus and method provide current limiting at power up without requiring the switching component to handle all operational current at all times. Further the apparatus and method allow operation of the device should the switching and/or the control circuit fail.

Brief Summary Text - BSTX (15):

These and other objects, features and advantages are achieved in a circuit and method which controls and limits the flow of in-rush current to a peripheral device coupled to a main power supply through a power bus and a ground bus. The circuit and method essentially isolate and limit in-rush current flow to a capacitor load of a peripheral device until the voltage across the load approaches voltage across the power supply. A switching device

US005886431A

United States Patent [19]

Rutigliano

[11] Patent Number: 5,886,431

[45] Date of Patent: Mar. 23, 1999

[54] **CIRCUIT AND METHOD OF OPERATION TO CONTROL IN-RUSH CURRENT FROM A POWER SUPPLY TO PERIPHERAL DEVICES IN AN INFORMATION SYSTEM**

[75] Inventor: **Jeffrey Paul Rutigliano**, Raleigh, N.C.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **935,781**

[22] Filed: **Sep. 23, 1997**

[51] **Int. Cl.**[6] **H02H 9/02**

[52] **U.S. Cl.** **307/131**; 323/908; 361/58; 395/283; 439/924.1

[58] **Field of Search** 307/119, 116, 307/146, 131; 361/58, 9; 395/283; 323/908; 439/924.1

[56] **References Cited**

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IBM Technical Disclosure Bulletin, vol. 36, No. 10, Oct. 1993, pp.335–340, entitled "Secondary Power Distribution Source for Point–of Sale Systems".

IBM Technical Disclosure Bulletin, vol. 32, No. 9B, Feb. 1990, pp.424–429, entitled "Hot–Plug Protection Circuit".

IBM Technical Disclosure Bulletin, vol. 24, No. 3, Aug. 1981, pp.1441–1442, entitled "Buck Converter with Switch Referenced to Ground".

IBM Technical Disclosure Bulletin, vol. 25, No. 2, Jul. 1982, p.470, entitled "Power Supply Inrush Current Limiter/Clamp Circuit".

Primary Examiner—Albert W. Paladini
Attorney, Agent, or Firm—John D. Flynn; Morgan & Finnegan

[57] **ABSTRACT**

This apparatus and method controls and limits the flow of in-rush current to a peripheral device coupled to a main power supply unit through a power bus and a ground bus. The apparatus and method essentially isolate and limit in-rush current flow to a capacitive load until operational current flow occurs to the peripheral device. A switching device is coupled to the power bus and the ground bus through a load. A resistive device is coupled to the power bus and the ground bus through the load. A control circuit is connected to the switching device. During initial start-up or "hot plugging" of the device, the control circuit turns "off" the switching device causing the load to be charged from the power bus through the resistive device until a predetermined condition occurs whereupon the switching circuit is turned "on" to bypass the resistive device and connect the load and the peripheral device to the power bus. Optionally, a uni-directional device may be connected between the power bus and the load to serve as a fail-charge/discharge path to the device in the event the switching device and/or the control circuit should fail. The apparatus and method provide current limiting at power up without requiring the switching component to handle all operational current at all times. Further the apparatus and method allow operation of the device should the switching and/or the control circuit fail.

9 Claims, 2 Drawing Sheets

US-PAT-NO: 5210855

DOCUMENT-IDENTIFIER: US 5210855 A

TITLE: System for computer peripheral bus for allowing hot extraction on insertion without disrupting adjacent devices

---------- KWIC ---------

Detailed Description Text - DETX (16):

The solution has been found to be sequentially connecting the grounds, power and data lines for controller cards exhibiting the delay of 0.015 sec. as indicated in the discussion for FIG. 4B. Thus as shown in FIGS. 4A and 4B, T0: would correspond to the ground interconnection; T1: the application of voltage from the bus; T1+0.015 sec. would correspond to voltage regulation to within 10% of nominal value; T2: would correspond to voltage regulation to within 1% of nominal value; and the interval T2-T1 would preferably be 0.090 sec. or approximately 6 times the 0.015 sec. interval. This is most easily implemented electronically by placing logic transmission gates or other suitable switches at all of the control circuit data line connections and delaying the enabling of those transmission gates until the voltage regulator has reached its steady state value and assumed a high impedance level. A time delay device controlling the switches would have to work properly during the entire power up operation, which could be to either the 10% or 1% nominal values. However, considerable real estate on the controller circuit board would be required to implement this solution. It may also cause difficulty in identifying and isolating the fault source in fault tolerant designs. A considerably simpler solution has been achieved by the careful utilization of the differential length connectors of the type used to implement normal hot plugging of peripheral devices with a fault tolerant bus.

US005210855A

United States Patent [19]

Bartol

[11] Patent Number: 5,210,855

[45] Date of Patent: May 11, 1993

[54] **SYSTEM FOR COMPUTER PERIPHERAL BUS FOR ALLOWING HOT EXTRACTION ON INSERTION WITHOUT DISRUPTING ADJACENT DEVICES**

[75] Inventor: Thomas M. Bartol, Hillsborough, N.C.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 957,746

[22] Filed: Oct. 7, 1992

Related U.S. Application Data

[63] Continuation of Ser. No. 364,743, Jun. 9, 1989, abandoned.

[51] Int. Cl.[5] G06F 13/00

[52] U.S. Cl. 395/800; 364/514; 364/DIG. 2; 395/325; 395/800

[58] Field of Search 395/500, 325, 800; 364/132, 514; 439/56, 59; 361/407, 413

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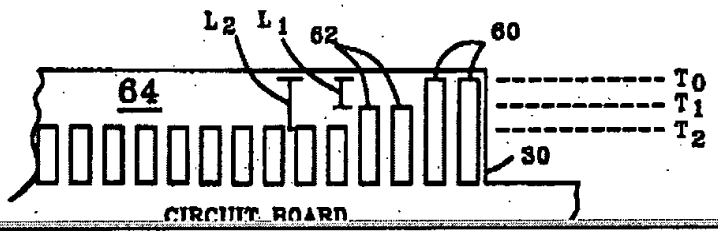
Primary Examiner—Thomas C. Lee
Assistant Examiner—L. Donaghue
Attorney, Agent, or Firm—Winfield J. Brown, Jr.; John C. Black

[57] ABSTRACT

A method and apparatus for rapid interconnection (hot plugging) peripheral device interface circuits to a computer bus is disclosed. The interconnections are completed using three sets of conductors in the sequence common grounds, power from the bus and data lines. The time period between the interconnections is determined by the relative set back lengths of the conductors from the card edge and allows for stabilization of voltage and establishment of a stable high impedance state for the peripheral device controller circuits before the data lines are interconnected.

6 Claims, 5 Drawing Sheets



L2: Entry 4 of 47 File: USPT Aug 13, 2002

DOCUMENT-IDENTIFIER: US 6434652 B1
TITLE: Hot plug subsystem for processor based electrical machine

Detailed Description Text (5):
When the Card 2 is plugged into the Socket 3 or removed from the Socket 3, the Controller 9 makes sure that even though the box is in full operational mode, the insertion or removal does not cause a deleterious effect on the box. For purposes of discussion, the signal bus is shown as two sections: namely, Box Signal Bus B and Card Signal Bus A. The Box Signal Bus B is coupled to Processor Base Subsystem 11 while Card Signal Bus A is coupled to Card Connector Socket 3. A similar structure is assigned to the power bus. In particular, the Box Power Bus D is connected to the Power Source 12 and the Card Power Bus C is connected to the Card Socket 3. The Hot Plug Sub-System 16 includes Card Bus Switch 4 coupled to the Box Signal Bus B and the Card Signal Bus A. The Card Bus Switch 4 provides the means of connecting and disconnecting the Card Signal Bus A to the Box Signal Bus B. When Card 2 is fully inserted in Card Connector Socket 3, the electrical continuity is maintained between the card, the Card Signal Bus A and the Box Signal Bus B if the card bus switch is in the closed state. If the switch is in the open state, there is electrical discontinuity between the Box Bus Signal B and the Card Signal Bus A. Preferably, the Card Bus Switch 4 should be of the type that has low on resistance without introducing propagation delay or additional ground bounce noise. Also, the switch may include a series termination resistor to reduce reflection in certain high speed applications. The prior art has several switches which can be selected for use. For example, Bus Switches QS32X2384 and QS32X2384, manufactured by QUALITY SEMICONDUCTOR, INC. are suitable candidates. The QS32X2384 includes internal 25 Ohm series termination resistors to reduce reflection noise in high speed application.

US Reference Patent Number (5):
5210855

L2: Entry 11 of 47 File: USPT Mar 13, 2001

DOCUMENT-IDENTIFIER: US 6202160 B1
**** See image for Certificate of Correction ****
TITLE: System for independent powering of a computer system

Detailed Description Text (71):
Referring to FIG. 5, the bias power portion of the remote interface board 104 will be described. As previously described, the independent RIB power supply 360, such as a 120 Volt AC/7.5 Volt DC power adapter, is connected to the DC power connector J2220. Pin 1 of the connector J2 connects via line 370 to provide the DC voltage to a VIN pin of the LT1376 high frequency step-down switching regulator 222. Pin 2 of the connector J2 connects to ground via line 372. The regulator 222, along with the external components suggested in the data sheet for the Linear Technology LT1376 component, provides a positive 5V output on a VCC5 line 374. The VCC5 line 374 connects to the other components on the RIB 104 to provide power to each RIB component. The VCC5 line 374 also connects to a fuse 224. In one embodiment the fuse 224 may be rated at 300 milliAmperes. The fuse 224 further connects via XVCC5 line 376 to pin 5 of RJ-45 connector 226, thereby providing 300 mA, positive 5V bias power to be fed to the server microcontroller network 102 (FIG. 1). The extender microcontroller bus clock (XLCL) and data (XLDA) signals to/from the switch 228 (FIG. 3) also connect to the RJ-45 connector 226 at pins 2 and 4, respectively. These signals correspond to I.sup.2 C clock and data signals.

US Reference Patent Number (28):
5210855

L2: Entry 32 of 47 File: USPT Dec 22, 1998

DOCUMENT-IDENTIFIER: US 5852743 A
TITLE: Method and apparatus for connecting a plug-and-play peripheral device to a computer

Brief Summary Text (14):
According to the present invention, one of the connector pins of the I/O port connector that have been defined as ground is used as a detection pin. The detection pin is connected to the system power supply Vcc through a resistor in order to maintain a high voltage level. The peripheral device has a matching connector that includes a pin corresponding to the detection pin. The corresponding pin is connected to ground. By detecting the voltage level at the detection pin, this invention can determine if a peripheral device is connected to the I/O port.

Detailed Description Text (2):
With reference to FIG. 1, the block diagram of the hardware architecture of this invention comprises a number of standard I/O interface connectors. One of the connector pins that have been defined as ground is selected as the detection pin A of each connector 1. The detection pin A maintains a high voltage level because it is connected to the system power supply Vcc through a resistor. The external device connector 2 on each peripheral device has a connection pin corresponding to the detection pin A. The corresponding connection pin on the external connector is grounded. When the peripheral device is connected to the system, the voltage level at the detection pin A drops to a low voltage level because its corresponding pin on the external connector is grounded.

US Reference Patent Number (1):
5210855

L2: Entry 44 of 47 File: USPT Dec 5, 1995

DOCUMENT-IDENTIFIER: US 5473499 A
TITLE: Hot pluggable motherboard bus connection method

Abstract Text (1):
A method of connecting an IC card to a motherboard involves first connecting the ground busses, then the power busses and finally the general signal busses. When the power busses are connected, a low current is allowed to flow initially, then, a predetermined period of time is allowed to elapse for equalization of IC card and motherboard voltages, then a full current is allowed to flow. A method of disconnecting an IC card from a motherboard involves first disconnecting the general signal busses, then the power busses and finally the ground busses.

Brief Summary Text (6):
In U.S. Pat. No. 5,210,855 to Bartol, for example, a connection sequence is described in which first ground connections are made, then power connections are made and finally general purpose signal connections are made.

Brief Summary Text (14):
A connector is provided on a motherboard for connecting the ground, power and general purpose signal connections of an IC card to the corresponding motherboard busses. During connection of an IC card to the motherboard, the connections are made in the following order. First, the ground connections are made, then the power connections are made, and finally the general purpose data connections are made.

Brief Summary Text (16):
When the IC card is to be removed from the motherboard, the connections between the IC card and the motherboard bus are disengaged in the reverse order from which they were engaged during the time when the IC card was being connected to the motherboard. That is, under programmed control, first the general purpose signal connectors are disengaged, then the power is disengaged and finally the ground connections are disengaged.

Detailed Description Text (2):
FIG. 1 shows a basic circuit structure of the present invention. An IC card 1 connects to a motherboard 2 via a connector circuit 21 located on the motherboard 2. The ground bus of the IC card 1 is connected to the ground bus 28 of the motherboard 2 during insertion of the card into connector 21. A controller 25 controls switches 22 and 23 located between connector 21 and general purpose signal bus 26 and power bus 27, respectively, so that the switches are closed as follows. When IC card insertion detector 30 detects that an IC card 1 has been physically inserted into a connector 21 by, for example, monitoring power supply current, (see FIG. 2 step S1), the controller 25 closes the switch 23 (steps S2 to S4 as will be fully described below) to connect the motherboard power bus 27 to the IC card 1. Finally, the controller 25 closes the switch 22 (step S5) to connect the motherboard general signal bus 26 to the IC card 1.

Detailed Description Text (5):
The controller 25 also controls the switches 22 and 23 in the following manner when IC Card removal initiator 40 detects that the user wishes to physically remove an IC card 1 from the motherboard 2 (see step S6 of FIG. 3). The switches are caused to open in a certain order, specifically, the reverse order to the order in which they were closed when the IC card was first connected to the motherboard connector 21.

More specifically, first the general signal bus switch 22 is opened (step S7), and then the power bus switch 23 is opened (step S8). Then, an indication is given to the user that it is alright to physically disconnect the card 1 from the motherboard connector 21 (step S9) by way of user signal 50. The ground connection is disconnected when the card is physically removed by the user.

US Reference Patent Number (10):
5210855

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L2: Entry 44 of 47 File: USPT Dec 5, 1995

US-PAT-NO: 5473499
DOCUMENT-IDENTIFIER: US 5473499 A

TITLE: Hot pluggable motherboard bus connection method

DATE-ISSUED: December 5, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Weir; Steven P.	Petaluma	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Harris Corporation	Melbourne	FL			02

APPL-NO: 08/ 083504 [PALM]
DATE FILED: June 30, 1993

INT-CL: [06] H02 H 9/00

US-CL-ISSUED: 361/58; 323/908, 395/750
US-CL-CURRENT: 361/58; 323/908, 710/302, 713/300

FIELD-OF-SEARCH: 361/58, 323/908, 395/750

PRIOR-ART-DISCLOSED:

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Search Selected | Search ALL

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ART-UNIT: 214

PRIMARY-EXAMINER: Deboer; Todd

ATTY-AGENT-FIRM: Sughrue, Mion, Zinn, Macpeak & Seas

ABSTRACT:

A method of connecting an IC card to a motherboard involves first connecting the ground busses, then the power busses and finally the general signal busses. When the power busses are connected, a low current is allowed to flow initially, then, a predetermined period of time is allowed to elapse for equalization of IC card and motherboard voltages, then a full current is allowed to flow. A method of disconnecting an IC card from a motherboard involves first disconnecting the general signal busses, then the power busses and finally the ground busses.

2 Claims, 3 Drawing figures

L7: Entry 19 of 21 File: USPT Dec 5, 1995

DOCUMENT-IDENTIFIER: US 5473499 A
TITLE: Hot pluggable motherboard bus connection method

Abstract Text (1):
A method of connecting an IC card to a motherboard involves first connecting the ground busses, then the power busses and finally the general signal busses. When the power busses are connected, a low current is allowed to flow initially, then, a predetermined period of time is allowed to elapse for equalization of IC card and motherboard voltages, then a full current is allowed to flow. A method of disconnecting an IC card from a motherboard involves first disconnecting the general signal busses, then the power busses and finally the ground busses.

Current US Cross Reference Classification (2):
710/302

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Search Results -

Terms	Documents
L5 and (ground same power same switch)	40

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DB=USPT; PLUR=YES; OP=OR			
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L7	L5 and (ground same power).ab.	21	L7
L6	L5 and (ground same power)	180	L6
L5	((710/301 |710/302)!.CCLS.)	556	L5
L4	(710/301,302.ccls.) and (power same ground)	0	L4
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 and (power same ground)	47	L2
L1	5210855.uref.	141	L1

END OF SEARCH HISTORY

L8: Entry 26 of 40 File: USPT Mar 9, 1999

DOCUMENT-IDENTIFIER: US 5881251 A
TITLE: Hot swap control circuit

Abstract Text (1):
A circuit board having a load is inserted into a chassis of a digital system while the system remains in operation. During insertion, a ground potential is provided to the circuit board. Next, one or more voltage potentials are provided, however, no electrical path is provided from the voltage potentials, through the load, to ground. An enhancement voltage is provided to the circuit board, allowing the load to charge. Finally, a backplane is connected to the circuit board after the load has charged. The circuit board includes a soft start circuit that allows the load to charge gracefully after the enhancement voltage is provided. In one embodiment, the soft start circuit includes an RC circuit connected to a switch which gradually turns on as the RC circuit charges, thereby providing an electrical path from the circuit board load to ground through the switch. The switch may be a MOSFET. Once the circuit board load is charged, connecting the backplane bypasses the MOSFET, thereby eliminating nearly all quiescent current flow through, and associated power dissipation in, the MOSFET. The circuit board is extracted from the chassis of the digital system by first disconnecting the backplane. When this occurs, the MOSFET is no longer bypassed by the backplane connection and quiescent current again flows through the MOSFET. Next, the enhancement voltage is removed, allowing the MOSFET to gradually turn off as the RC circuit discharges, thereby removing the electrical path from the load to ground. The voltage and ground potential are then removed.

Brief Summary Text (10):
The circuit board includes a soft start circuit to allow the circuit board to charge gracefully after the enhancement voltage is provided. In one embodiment, the soft start circuit includes an RC circuit which charges over a predetermined time after the enhancement voltage is provided. The RC circuit is connected to a switch which gradually turns on as the RC circuit charges, thereby providing an electrical path from the circuit board load to ground through the switch. In one embodiment, the switch is a MOSFET having a current rating appropriate to the quiescent circuit board load current. Once the circuit board load is charged, connecting the backplane bypasses the MOSFET, thereby eliminating nearly all current flow through, and associated power dissipation in, the MOSFET.

Detailed Description Text (3):
FIG. 1 illustrates a digital system 5 configured in accordance with the present invention. Digital system 5 includes a chassis 10 and a circuit board 20. Chassis 10 includes a ground post 30, power posts 31, a soft start post 32, and a backplane connector 33. Circuit board 20 includes a ground connector 40, power connectors 41, a soft start connector 42, a backplane coupling 43, a switch circuit 50, and board loads 60. Circuit board 20 may be inserted into or extracted from chassis 10 at any time, without having to power down the digital system 5.

Detailed Description Text (4):
In one embodiment, chassis 10 is configured so that ground post 30 will make contact with ground connector 40 as circuit board 20 is inserted into chassis 10 before any other electrical connections between circuit board 20 and chassis 10 are established. For the embodiment shown in FIG. 1, this is accomplished by making ground post 30 longer than power posts 31, soft start post 32 and backplane connector 33. Power posts 31, and soft start post 32 are approximately the same

length. Circuit board 20 is configured such that ground connector 40 and power connectors 41 are situated on the leading edge of circuit board 20. Soft start connector 42 is recessed a desired distance from the edge of circuit board 20. The recess distance will depend upon the charge and discharge time of switch circuit 50. In one embodiment, soft start connector 42 is recessed a distance of 0.2" from the leading edge of circuit board 20.

Detailed Description Text (5):
Insertion of circuit board 20 into chassis 10, should be carried out in a controlled manner. Ground post 30 on chassis 10 is first coupled with the ground connector 40 on circuit board 20 in order to facilitate electrostatic discharge of the circuit board 20. Next, power post(s) 31 on chassis 10 is/are coupled with power connector(s) 41 on circuit board 20. Each power connector 41 is coupled to a respective circuit board load 60. Circuit board loads 60 represent the equivalent circuit loads for the various circuits located on circuit board 20. Notice that even though power posts 31 are connected to power connectors 41, no current flows across circuit board loads 60 because switch circuit 50 acts as an open circuit, preventing a path from the circuit board loads 60 to ground.

Detailed Description Text (7):
As MOSFET 52 switches on, circuit board loads 60 are provided with a path to ground post 30. Those skilled in the art will recognize that MOSFET 52 is current rated depending upon the magnitude of the quiescent circuit board loads 60. After circuit board loads 60 are charged, and as circuit board 20 is further inserted into chassis 10, backplane connector 33 on chassis 10 is coupled to backplane coupling 43 on circuit board 20. Backplane coupling 43 on circuit board 20 and backplane connector 33 on chasis 10 provide a current path which bypasses MOSFET 52. As a result, even though MOSFET 52 remains turned on, there is little or no further power dissipation in MOSFET 52.

Detailed Description Text (8):
Extraction of circuit board 20 from chassis 10 should also be carried out in a controlled manner. During extraction, backplane connector 33 is first disconnected from backplane coupling 43 and quiescent current again begins to flow through MOSFET 52 to ground post 30. As extraction of circuit board 20 continues, soft start post 32 is disconnected from soft start connector 42. Disconnecting soft start post 32 in this fashion causes RC circuit 54 to discharge through resistor circuit 56, allowing circuit board load 60 to power down gracefully as MOSFET 52 switches off. As the extraction process continues, power posts 31 are disconnected from power connectors 41, removing all voltage from circuit board 20. After power posts 31 are disconnected, ground post 30 is disconnected from ground connector 40, completing the extraction of circuit board 20 from chassis 10.

Detailed Description Text (9):
FIG. 2a illustrates an alternative embodiment of digital system 5. In this embodiment, chassis 10 is again configured so that ground post 30 is longer than power posts 31 and soft start post 32. However, power posts 31, and soft start post 32 are of different lengths. Soft start post 32 is shorter than power posts 31. The measure of distance between the length of power posts 31 and soft start post 32 again depends upon the charge and discharge time of switch circuit 50. With this embodiment, ground connector 40, power connectors 41, and soft start connector 42 may all be situated on the leading edge of circuit board 20. The provision (during insertion) or removal of the various potentials will occur in the same sequence as that described above as circuit board 20 is inserted or extracted from chassis 10 despite the different physical configuration.

Current US Original Classification (1):
710/302

CLAIMS:

12. A method of removing a circuit board having a circuit board load from a chassis comprising the steps of:

disconnecting a backplane from the circuit board;

removing an enhancement voltage from the circuit board by terminating a quiescent current flow from the circuit board load through a switch to an electrical ground in a controlled fashion, the circuit board thus being configured to allow the circuit board load to power down gracefully once the enhancement voltage is removed;

removing one or more voltage potentials from the circuit board once the circuit board load has powered down; and

removing a ground potential from the circuit board only after all other voltage potentials have been removed therefrom.

L8: Entry 37 of 40 File: USPT Dec 5, 1995

DOCUMENT-IDENTIFIER: US 5473499 A
TITLE: Hot pluggable motherboard bus connection method

Detailed Description Text (2):
FIG. 1 shows a basic circuit structure of the present invention. An IC card 1 connects to a motherboard 2 via a connector circuit 21 located on the motherboard 2. The ground bus of the IC card 1 is connected to the ground bus 28 of the motherboard 2 during insertion of the card into connector 21. A controller 25 controls switches 22 and 23 located between connector 21 and general purpose signal bus 26 and power bus 27, respectively, so that the switches are closed as follows. When IC card insertion detector 30 detects that an IC card 1 has been physically inserted into a connector 21 by, for example, monitoring power supply current, (see FIG. 2 step S1), the controller 25 closes the switch 23 (steps S2 to S4 as will be fully described below) to connect the motherboard power bus 27 to the IC card 1. Finally, the controller 25 closes the switch 22 (step S5) to connect the motherboard general signal bus 26 to the IC card 1.

Detailed Description Text (5):
The controller 25 also controls the switches 22 and 23 in the following manner when IC Card removal initiator 40 detects that the user wishes to physically remove an IC card 1 from the motherboard 2 (see step S6 of FIG. 3). The switches are caused to open in a certain order, specifically, the reverse order to the order in which they were closed when the IC card was first connected to the motherboard connector 21. More specifically, first the general signal bus switch 22 is opened (step S7), and then the power bus switch 23 is opened (step S8). Then, an indication is given to the user that it is alright to physically disconnect the card 1 from the motherboard connector 21 (step S9) by way of user signal 50. The ground connection is disconnected when the card is physically removed by the user.

Current US Cross Reference Classification (2):
710/302

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☐ 1. Document ID: US 6560750 B2

L4: Entry 1 of 6 File: USPT May 6, 2003

US-PAT-NO: 6560750
DOCUMENT-IDENTIFIER: US 6560750 B2

TITLE: Method for providing master-slave heat-swapping apparatus and mechanism on a mono-ATA bus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 6529987 B1

L4: Entry 2 of 6 File: USPT Mar 4, 2003

US-PAT-NO: 6529987
DOCUMENT-IDENTIFIER: US 6529987 B1

TITLE: Hot pluggins in a PCI bus system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 6269416 B1

L4: Entry 3 of 6 File: USPT Jul 31, 2001

US-PAT-NO: 6269416
DOCUMENT-IDENTIFIER: US 6269416 B1

TITLE: Adaptive PCI slot

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 4. Document ID: US 5886431 A

L4: Entry 4 of 6 File: USPT Mar 23, 1999

US-PAT-NO: 5886431
DOCUMENT-IDENTIFIER: US 5886431 A

TITLE: Circuit and method of operation to control in-rush current from a power supply to peripheral devices in an information system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw Desc | Image

☐ 5. Document ID: US 5758102 A

L4: Entry 5 of 6 File: USPT May 26, 1998

US-PAT-NO: 5758102
DOCUMENT-IDENTIFIER: US 5758102 A

TITLE: Soft switching circuit for use on backplane

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 6. Document ID: US 5210855 A

L4: Entry 6 of 6 File: USPT May 11, 1993

US-PAT-NO: 5210855
DOCUMENT-IDENTIFIER: US 5210855 A

TITLE: System for computer peripheral bus for allowing hot extraction on insertion without disrupting adjacent devices

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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l1 and L3	6

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